Design and Test of an ATLAS ITk Multi-Pixel Module Test Stand

Thesis submitted in partial fulfillment of the requirements for the degree of
Master of Science in Physics

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Contents

1 Introduction

This thesis is part of Siegen's work for CERN's (from fr. Conseil Européen pour la Recherche Nucléaire) A Toroidal LHC Apparatus (ATLAS) project. It contains an introduction to the physics and research/experimental environment of the subject of the thesis, the design requirements and how they were fulfilled during the building and commissioning of the test stand, as well as a description and explanations of the hardware and software involved in running the test stand.

The design and testing of a new test stand were necessary, since the envelope and connections of the new modules exclude the existing test stands from the first pixel assembly. The testing environment is required to be dust free, dry and have the capability of cooling the module to the required testing/operating temperatures. In addition to this, the test stand needed to be automatable to allow for the expected module flow of four modules a week, and include all the safety systems required by the ATLAS collaboration.

1.1 LHC

The Large Hadron Collider (LHC) is a particle accelerator ring at the border between France and Switzerland. It was built into the preexisting tunnels of the Large Electron Positron Collider. Two additional experimental caverns were dug to house the experiments of ATLAS and CMS, whereas LHCb and ALICE were built into existing caverns. The collider sits at a minimum depth of 50 meters underneath the earth and has a circumference of 26.659 km [1].

It accelerates two proton beams from the initial injection energy of 450 GeV to a maximum planned energy of 7 TeV per beam leading to a center-of-mass (COM) energy of 14 TeV. In May 2015, the accelerator reached a collision energy of 13 TeV. The current highest achieved collision energy is 13.6 TeV, since April 2022. At these energies, the protons move at approximately the speed of light, which, with the circumference of the accelerator, corresponds to a revolution frequency of about 11 kHz. When fully filled, the ring is designed to accelerate 2800 proton packets called bunches, each containing around 10^{11} particles. This, along with a gap in the bunches to allow for controlled ejection of the beams, creates a theoretical

collision frequency of 40 MHz or one bunch crossing every 25 ns. The real collision frequency is slightly lower as the structure of the proton bunch and the luminosity profile of the beams allow for a bunch crossing resulting in no collision.

Each of the four mentioned experiments focus on different aspects of the collision products: ATLAS and CMS are multi-purpose detectors that use different detection equipment allowing to confirm each other's measurements. ALICE is designed to examine the high-energy environment generated in heavy-ion-collisions during alternative runs of the LHC with lead ion beams or, in future, proton–lead or proton–oxygen collisions [2]. LHCb concentrates on b-quark measurements in the forward direction of the collisions.

The maximum COM energy is planned to be reached during Run 4 in 2029, after extensive upgrades to the linear and pre-accelerator rings as well as upgrades to the ATLAS and CMS experiments, to handle the increased luminosity from both, the increased collision energy, as well as planned increases in the density of the proton bunches. The current level of pileup (proton–proton collisions per bunch crossing) is at around 60 and is expected to reach up to 140 [3] for the high luminosity LHC development phase. The following section will outline the relevant upgrades necessary for ATLAS to handle the LHC upgrade to its high luminosity phase.

1.2 ATLAS

The ATLAS detector started operations in 2008. Among the more than 1000 physics publications, the most prominent was the discovery of the Higgs boson in 2012 [4], independently of the measurements taken by CMS. ATLAS is shaped as a 46 m long cylinder with a diameter of 25 m and a mass of about 7000 t. The detector (see figure 1.1) is built in onion-like layers with four main components [5]:

1) Magnet system (MS): The superconducting magnet system generates the necessary magnetic fields for the other detection systems. This allows the direct measurement of the charge and momentum of the charged particles generated in the collision via the tracking detectors. The MS is split into two parts. The central solenoid supplies the field for the inner detector and the air-core toroids provide the magnetic field for the muon spectrometer.

2) Inner detector: It is made of 3 different detection systems for tracking charged particles, decreasing in resolution with increased radius. The innermost system is the pixel detector consisting of cylindrical layers plus 3 endcaps on each side. Layered around the pixel detector, are 4 cylindrical layers of silicon strip detectors with 9 endcap discs on each side. Finally, enclosing the strip detector is the transition radiation tracker (TRT). In a recent upgrade, the beam pipe going through the detector was shrunk to allow for a 4th layer to be inserted into the pixel detector. This insertable B-layer (IBL) was installed in 2014 [6].

3) Calorimeter system: The system consists of an electromagnetic calorimeter and a hadronic calorimeter to measure the energy of the produced particles. The electromagnetic calorimeter uses liquid argon and lead as the detector material. The hadronic calorimeter is scintillator-based, using a sampling calorimeter with higher Z materials as a shower medium. Steel is used in the barrel section of the calorimeter and copper and tungsten are used in the forward regions.

4) Muon detector: The muon detector consists of two parts. One for high-precision measurements of the muons in position and momentum. The other, used as part of the trigger system for data readout.

The systems of the ATLAS detector were designed for 23 pileup interactions per bunch crossing at LHC design luminosity. They were built to last until the end of Run 3 of the LHC, after which the inner detector would reach its limitation due to radiation damage. The current running of the detector beyond design is only possible due to the mentioned IBL upgrade and better tracking algorithms. As such, the plans to increase the luminosity in LHC Run 4 and beyond require an upgrade to the ATLAS systems to deal with up to 140 pileup [3] events per bunch crossing. The main upgrade is the fully silicon inner tracker (ITk), which is planned to replace the inner detector as described in the next section.

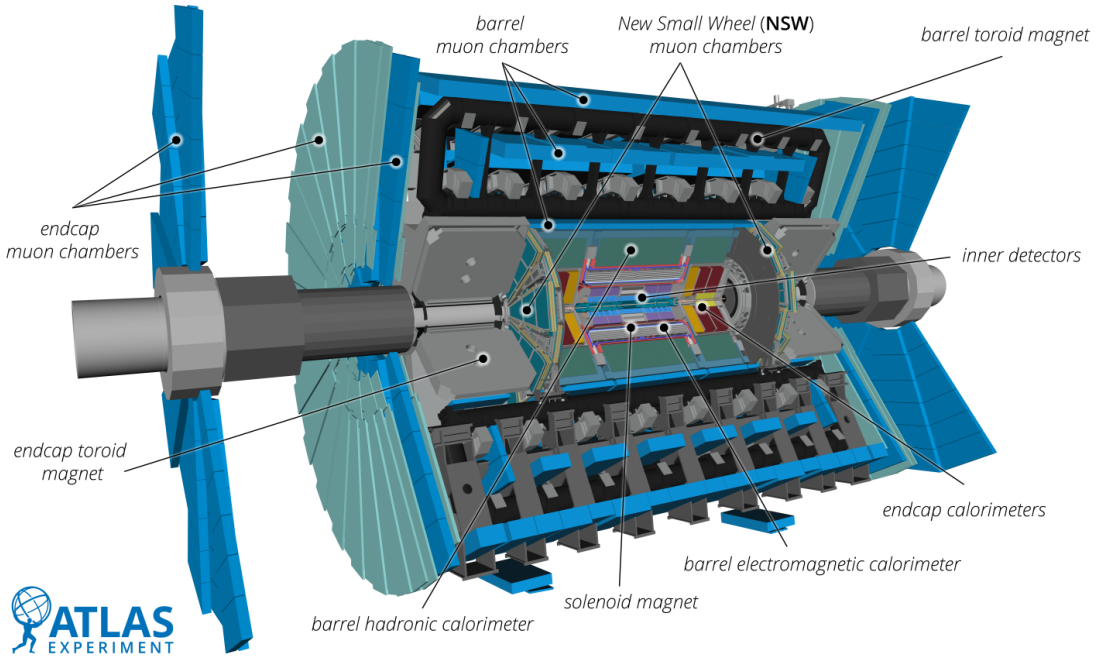

Figure 1.1: ATLAS schematics with labels [7].

1.3 Inner tracker

The inner tracker is the replacement project for the radiation-damaged and outdated inner layers of the current ATLAS detector. They will be replaced by a fully silicon-based detector system divided into two conceptual layers. The outer layer is the silicon strip detector and the inner layer is the new pixel detector. The pixel detector can be divided again into an inner system and an outer barrel. The inner system, consisting of pixel layers 0 and 1, is strongly constrained in volume as it is close to the beam pipe of the LHC. This is why various module types and architectures are employed in these layers. The inner system is also designed to be easily replaceable since the projected radiation dose in these layers will exceed the lifetime of the readout chips after half of the expected detector operation. Due to the volume limitation, the inner layers use a single wide module configuration for readout, with single, double, or triple chips in length, parallel to the beam pipe. The outer system will be exclusively built with quad modules in a 2×2 chip configuration. Each module covers an area of about $40 \times 42\,\mathrm{mm}^2$ with an active

sensor area of $40 \times 41\,\mathrm{mm}^2$ divided into 768×800 pixels of mostly $50 \times 50\,\mu\mathrm{m}^2$ size. Pixels bridging gaps between two readout chips are merged to allow recovering of signals deposited in the gap. The readout chips are variations of the RD53 design with the current pre-production modules built with RD53b (also called ITkPixV1 [8]) and RD53c (ItkPixV2 [9]) chips. The outer system comprises 3 barrel layers and 8-10 end-cap rings. The Inner Tracker is expected to generate up to 19 hits for a perfect track in the detector and will consist of around $14\,\mathrm{m}^2$ for the pixel tracker and around $165\,\mathrm{m}^2$ for the strip detector [10][11][12].

1.4 The Outer Barrel quad module

The Outer Barrel quad module is a hybrid pixel detector meaning that the sensor and readout electronics are created on separate objects and later connected via conducting material. The 614400 (800×768) pixels of the silicon pixel detector are connected via individual SnAg bump bonds to the four RD53-based readout chips. This creates what is referred to as a bare module. These bare modules and the corresponding flexible printed circuit boards (Flex) are mated with epoxy glue inside a special gluing tool and process. The Flex is attached to the top of the sensor via the glue and the chips and sensor are electrically connected to the Flex via around 800 12.5 μm aluminum wire bonds. This described package is then mounted in the module carrier (MC), see figure 1.2.

The MC is made of four parts plus screws to keep it together. From the bottom, one has the base plate, with a specifically made shape to enforce the correct orientation during carrier assembly and a polished surface, on which the module rests with the bottom of the readout chips. Next, are two halves of the main carrier. The frame of the Flex is held between the two halves. The halves are kept together with four M1 Phillips screws in the corners and can be secured to the base plate with two M3 screws for storage and travel. Additionally, the top half of the main carrier contains fixtures to hold onto the flat band cables necessary for electrical testing. The last part of the carrier is the cover, that protects the inside from small objects and dust. The cover also holds structures to lightly press the flex against the bottom of the carrier to secure it from damage via vibration or shock. The cover is held to the main carrier via two thumb screws.

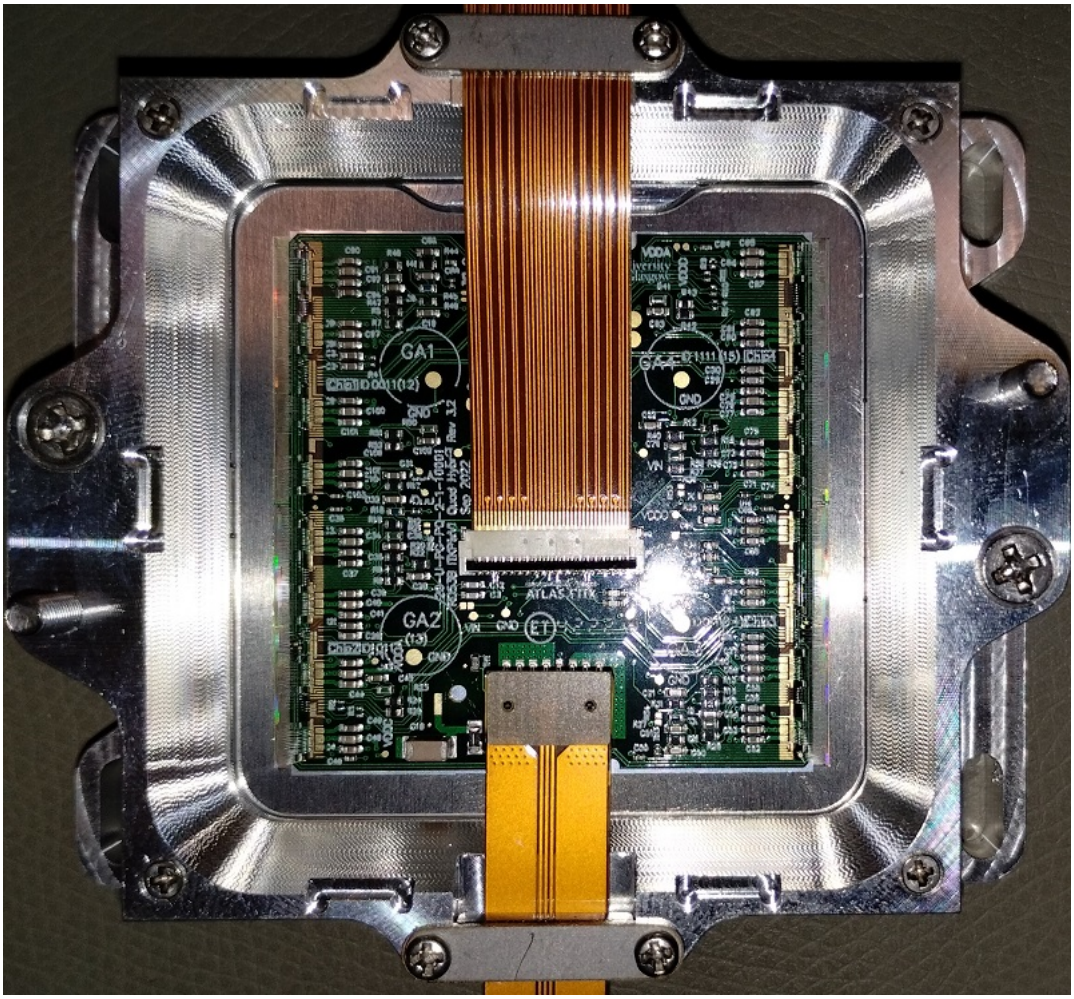

Figure 1.2: ITk pixel quad module in a module carrier (cover removed).

1.5 Readout chip

The RD53 readout chip physical size is $20 \times 21\,\mathrm{mm}^2$ with the active pixel array being $20 \times 20\,\mathrm{mm}^2$. The array of 400×384 pixels is split into 50×48 pixel cores. Each core (8×8 pixel) is further split into 2×8 pixel regions of 1×4 pixel size. Each pixel region handles leading edge detection, and TOT (time-over-threshold) charge information with 8 shared latency buffer registers. Each pixel of the sensor is connected to a bump bond pad on the surface of the chip and internally connected to an analog front-end (AFE). The AFE handles analog calibration charge injection and pixel-specific configuration. It handles four pixels in a 2 by 2 configuration. This means two-pixel regions (1×4) stacked on top of each other are made of 2 AFEs side by side. The columns of the AFE are connected for analog biasing with each column, having dedicated bias drivers and connecting to the analog chip bottom (ACB). The ACB also handles analog digital conversion (ADC), calibration, biasing digital to analog conversion, command decoding register, phase-locked loop, and various sensors. To do so, it is connected to the digital chip bottom, which handles the digital side of the sensors, the digital communication to the outside, and their driver/ receivers. To interact with the outside world, the chip has the pad frame at the bottom. It handles connections for ESD protection, SLDO power regulators, and the IO pads for the chip [8].

1.6 Physics aspects and considerations

1.6.1 Solid state detectors

The sensor of the quad module relies on an efficient solid-state ionization. This physics principle allows moving charges (electron hole pairs) to be created by particles passing through a depleted semiconductor [13]. The charged particle passing through the material loses energy via ionization as described by the Bethe Bloch-equation:

$$-\langle\frac{dE}{dx}\rangle = \frac{4\pi}{m_e c^2}\frac{nz^2}{\beta^2}\left(\frac{e^2}{4\pi\epsilon_0}\right)^2\left[\ln\left(\frac{2m_e c^2\beta^2}{I(1-\beta^2)}\right) - \beta^2\right]. \tag{1.1}$$

In the case of the quad module sensor, the depletion voltage applied to the diode is low enough (120 V initial, up to 1 kV at end of lifetime) not to cause cascading

effects but high enough to fully deplete the thin (100μm) sensor and allow for quick charge separation inside. The sensor funnels generated electrons to the readout chips via the reception pads and bump bonds. In the readout chip, charge-sensitive amplifiers amplify the signal to usable levels.

In its main detection mode, this sensor is sensitive to any charged particle passing through it, as they leave a wake/streak of electron hole pairs on their trajectory. The secondary mode of detection relies on the interaction between electromagnetic (EM) radiation and the detector material. X-rays and gamma radiation can knock an electron loose at high enough energy to be detected. The number of electron hole pairs generated is proportional to the energy lost by the charged particle. To create an electron hole pair in silicon at room temperature, an energy of ~ 3.6eV is necessary. The energy loss of a minimum ionising particle is about $2\,\mathrm{MeV}\cdot\mathrm{cm}^2/\mathrm{g}$ and combined with a sensor thickness of 100 μm and the density of silicon of $2.33\,\frac{\mathrm{g}}{\mathrm{cm}^3}$ one can estimate the number of generated electron-hole pairs:

$$n_{e^-} = 2\,\frac{\mathrm{MeV}\cdot\mathrm{cm}^2}{\mathrm{g}} 2.33\,\frac{\mathrm{g}}{\mathrm{cm}^3} 0.01\,\mathrm{cm}/3.6\,\mathrm{eV} \approx 12778. \tag{1.2}$$

Our sensor generates about 12778 electron hole pairs for a perpendicular pass-through. The readout chip is capable of detecting as low as 800 electrons in one pixel with nominal tuning being 1500 electrons. This allows for grazing hits to be detected, as well. The holes are sinked/recombined at the source of the depletion voltage, while the electrons slowly (see TOT) flow into the chips ground.

1.6.2 Isolation/ heat transfer equation:

One of the main functions of the test stand is generating and maintaining the testing temperature. To achieve this, the outside needs to be isolated from the inside. A source/sink of thermal energy needs to be present inside the test stand and it needs to be thermally connected to the test object. The physics problem of thermodynamics is generally complex and dependent on the geometry and materials involved. We assumed a static load/system for all equations and simplified them to a problem of heat transfer through a plane of thickness x and material y with the temperature gradient of δT. The following equation then describes the

energy flux of this static system:

$$q(x, y, \delta T) = -k_y \frac{\delta T}{x}. \tag{1.3}$$

In a stable state, the temperature difference between the outside of the test stand and the inside can reach up to 60° C. We want as little energy transfer as possible. Therefore the thermal conductivity k of the material providing the thermal barrier needs an as smal value of k as possible. 2 cm thick styrodure sheets (polyurethane foam $k = 0.032\,\mathrm{W/(m \cdot K)}$) were chosen, as they are cheap, light, strong, and easy to work with. The inverse is true for all materials that are in thermal contact with the quad module, as we want δT to be as small as possible for stability and control. Aluminum ($k = 237\,\mathrm{W/(m \cdot K)}$) for the bulk material was chosen, due to its availability, price, and manufacturability. Copper ($k = 401\,\mathrm{W/(m \cdot K)}$) would have been another possible choice. The price, hardness, and tendency to corrode into a water-soluble material make, it problematic for a cooling plate,which is to be cooled by a water-ethanol solution. Equation 1.3 works for stacked systems, but calculating k for contact layers is practically impossible since the contact area between materials is never flat. Because of this, the temperature gradient between the active quad module and the cooling plate is largely dependent on the quality of contact between the different stacked layers of the system (see figure 1.3):

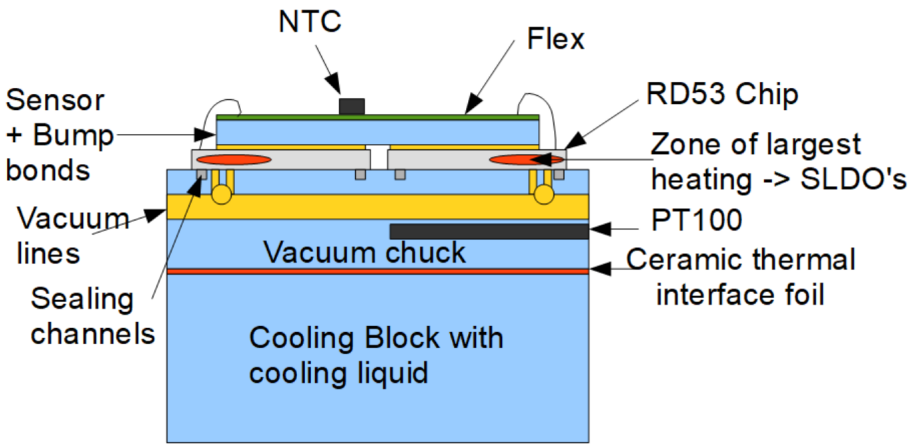

Figure 1.3: Schematic thermal layers inside the test stand.

Chips (silicon) $\Longrightarrow$ Contact1 + vacuum $\Longrightarrow$ Vacuum chuck (aluminum) $\Longrightarrow$ Thermal interface foil $\Longrightarrow$ Cooling plate (aluminum) $\Longrightarrow$ Liquid interface to chiller. The air temperature can be ignored, since a cold flat horizontal surface in contact with air has practically no heat exchange due to convection, the air being a strong insulator ($k \approx 0.025\,\mathrm{W/(m \cdot K)}$). This all results in a measured δT of 6° C when the cooling liquid is at 14° C for one active module or 7° C for four active modules in the test stand. At cold temperatures of −24° C, the temperature is offset to $9 - 10°$ C for the active quad modules. The increased offset at lower temperatures can be explained by the extra heat transfer to the dry air system. Since it is also routed through the cold plate and the δT to room temperature for the dry air is around 45° C. The undersized cooling channels in the cooling plate cause this effect to be less visible at higher coolant/ smaller gradient temperatures.

1.6.3 Sr^{90} electron source

Strontium 90 is a radioactive isotope. It is produced in the decay chain of uranium 235 fission products with the atomic weight of 90 such as krypton 90 or bromine 90. Br^{90} decays with a half-life of 1.91 s into Kr^{90} via beta decay. Kr^{90} decays into rubidium 90 with a half-life of 32.32 s and Rb^{90} decays with a half-life of 158 s into Sr^{90} [14]. As all the mentioned isotopes have a far shorter half-life than the half-life of Sr^{90} with 28.78 a, it accumulates in the burned-out fission fuel, from which it can be extracted. Sr^{90} decays into Y^{90} via beta decay with a maximum energy of the electron being 546 keV. The daughter yttrium decays relatively quickly with a half-life of 64 h via beta decay with 2.282 MeV maximum energy.

As beta decay is a three body decay, the generated energy spectrum of the resulting electron is continuous with an average electron energy of about 1/3 of the maximum decay energy. This leads to a continuous spectrum for the Sr^{90} and Y^{90} decays, with two peaks at 180 keV and 760 keV. According to the integrated energy loss function, the maximum decay energy of 2.282 MeV results in a maximum range in aluminum [15] of 4 to 5 mm. As such, the shielding of the source needs to be at least 5 mm thick.

2 Design and development

2.1 Requirements

The following requirements directly derive from a set of fixed requirements from the ATLAS testing documents [16][17][18][19][20][21][22] and from the optimal use of local resources.

The test stand needs to house and control up to four ITk outer barrel quad pixel modules. The module NTC needs to be kept at -15° C $\pm$ 3° C during cold testing in a powered state. The modules need to be attached to the cooling block with a vacuum of at least δp of -500 mbar. The vacuum seal to the chips needs to be made with silicon rubber, to ensure no residuals on the backside of the chips. Dry air needs to be supplied constantly and has to be oil-free and filtered with a HEPA filter for dust. The dew point provided by the dry air system needs to be at least 5° C lower than the NTC temperature of the modules. The stand has to include an environmental monitoring sensor for relative humidity, air temperature, and dewpoint, temperature sensors for each vacuum chuck, a lid/closure switch, and dry air and vacuum sensors for the DCS/interlock system. The stand needs an automated way of moving a radioactive source from a protected garage to positions above the modules to allow for self-trigger testing of the modules. Lastly, the modules should be easily accessible and the box should be sealed as air-tight as possible to reduce dry airflow and cooling requirements.

2.2 Periphery

Several external devices are required in order to operate the test stand.

First, the devices chosen for environment control are a Julabo FP51 SL chiller running an 80/20 mixture of ethanol and water to achieve a possible freezing point below -35° C, and a compressed air dryer (OFP SMART 0010 Superplus) to supply up to 15 l/min of -75° C dew point air to the system. To supply power and data to the modules, four data and power adapter boards are needed. The power supply units for low voltage (Rohde & Schwarz HMP 4040) and for high voltage (Keithley 2470 SourceMeter) are connected to these adapters. The module data is read out via a YARR (Yet Another Rapid Readout) controlled commercial

Trenz Electronics FPGA card (TEF 1001 R2) in the readout/control PC. Module voltages from the chip's voltage multiplexer outputs are read out with a digital multimeter (Keithley DMM 6500) via a 10-channel multiplexer card installed in the multimeter see figure 2.1.

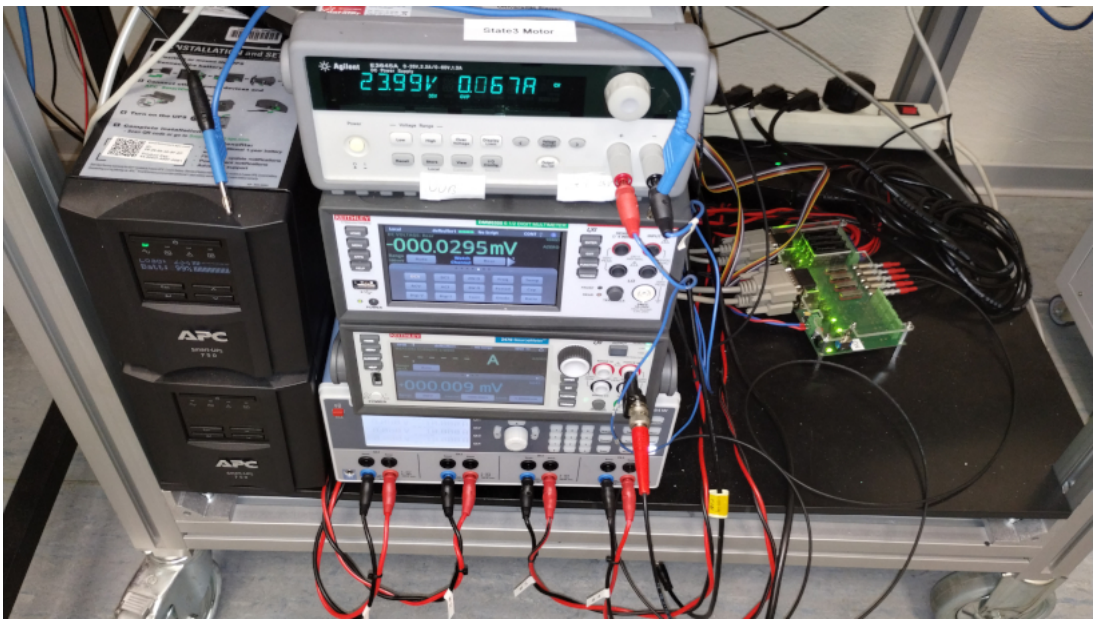

Figure 2.1: Periphery stack an the cRIO relay card.

The last three periphery pieces are the source movement system, the hardware interlock based on the commercial cRIO system, and the Interlock/device control PC, which are described later.

2.3 Cooling plate

The cooling plate is meant to hold four vacuum chucks, each holding a module via vacuum. The whole cooling assembly has to dissipate up to 64 W of electrical heating from the four modules, plus a theoretical 250 W of thermal power from the dry-air cooling to the cooling liquid. The dry air cooling power number comes from a flow estimate of 1 m of dry air tube per second with the tube inner diameter being around 3 mm. This leads to a mass flow of $3.66\,\mathrm{g}/s$ of dry air at room temperature and pressure ($\rho_{\mathrm{air}} = 1.293\,\mathrm{kg/m^3}$). The specific heat capacity of air under constant

pressure is $c_p = 1.005\,\mathrm{kJ/(kg \cdot K)}$ and the temperature difference being 60 K. This leads to an estimated thermal load of $P = \frac{m}{\Delta t}\delta T \approx 0.22\,\mathrm{kJ/s} = 220\,\mathrm{W}$. This initial estimate was increased to 250 W to match with the replaced air in the testing volume ($0.002\,\mathrm{m}^3$) every 6.25 seconds. The plate is manufactured from a 480 mm by 84 mm by 12 mm block of aluminum (see figure 2.2).

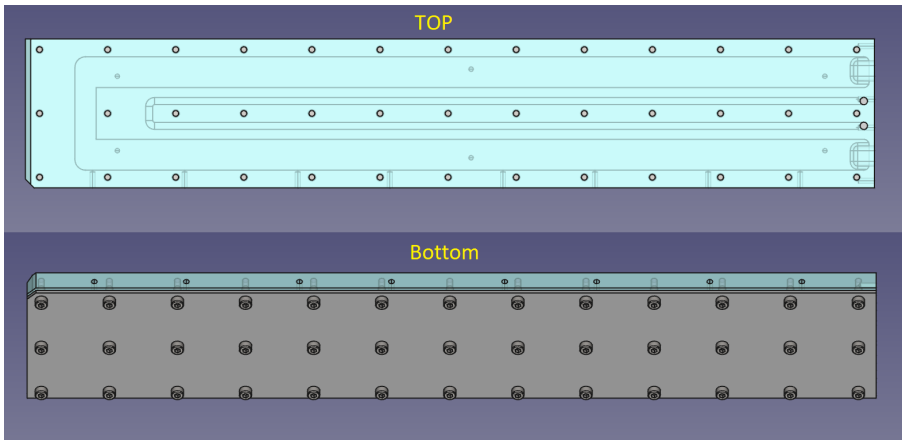

Figure 2.2: CAD design of the bare cooling plate made partially transparent.

An array of 39 (13x3) M4 threaded holes makes the basis of both the mounting system for the vacuum chucks as well as holding the silicone rubber sealing sheet and the 2mm thick aluminum cap via 39 M4x10 hex cap screws on the bottom side. From the bottom side, two U-shaped channels were milled into the metal block. The thicker outer channel (17.5 mm width and 6 mm depth) is for the cooling fluid and has cooling fins integrated into the long arms of the U-shape. The top parts of this U are connected to the outside via an oval pass-through hole in the smaller side face, to which two adapter pieces are mounted via two M4x10 screws each. These adapters join the plate to the cooling loop via two 90° Festo L-connectors with one side being G1/2 thread and the other a Festo 12 mm tubing connector. The second inner U-shaped channel (4 mm width and 4 mm depth) is for cooling incoming dry air/nitrogen and is connected to the outside via two 45° holes to the top side of the plate on the same end as the cooling adapters. These holes are threaded with M4 threads and cut-outs on the top face are in place to fit two M4 to 4 mm tubing straight Festo connectors which connect to the dry air/nitrogen system.

2.4 Vacuum chucks

The Vacuum chuck (VC) is machined out of an aluminum block, 60 mm long by 84 mm wide by 13 mm high. Most of the block is milled down to 10 mm thickness. Only the contact surface, which matches the bottom of the module carrier, is left at 13 mm to ensure good contact with the module suspended in the carrier top. This contact surface has 4 seal grooves cut in rounded squares underneath the chip positions. A groove is high and wide enough to fit a 1.5 mm diameter medical silicone tubing, which acts as the seal. Along the inner edges of these grooves, an L-pattern of holes is placed, so that they form a square with the short leg of the L pointing inwards. This ensures that the vacuum pulls the end of chip/wirebond area to the VC's surface for thermal contact . This area has the chip's highest thermal load due to the presence of the chips SLDO presence (figure 2.3).

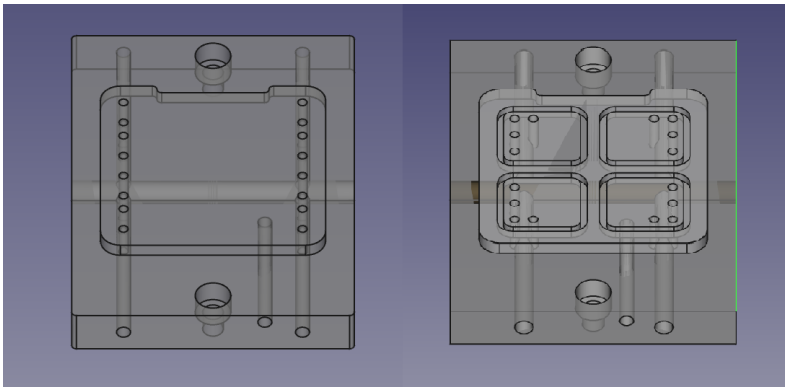

Figure 2.3: CAD designs of the old/new vacuum chuck made partially transparent.

The seals underneath the chips ensure maximum thermal contact. Should the module buckle under thermal stress then the area of vacuum increases along with the pressure pushing the module to the surface. During a test of a previous version of the VC, without the seals, the module lost vacuum and therefore thermal contact, leading to a test shutdown at -5° C module temperature. This prompted a redesign as the modules need to be tested at -15° C.

The vacuum holes under the chips are joined via two 4 mm horizontal channels filled in at the ends to be airtight. The two connection holes are joined via the main 6 mm-wide vacuum conduit, which is threaded at both ends to allow for the attachment of the M6-to-Festo 6 mm adapter to the vacuum system. At the

top and bottom of the VC are sunk-in attachment structures designed to receive M4x10 hex screws. The distance between them match the hole pattern of the cooling plate. The VCs, when attached to the cooling plate, are spaced 115 mm apart from each other to allow for up to four VCs to be mounted on the plate.

2.5 Isolation box

The isolation box housing the modules and the cooling plate was built by first stacking three sheets of 2 cm-thick Styrodur, fused with non-foaming polyurethane (PU) glue. In the second step the workshop cut the stacked sheets to size and milled out the indent which will hold the cooling plate and its connection (see figure 2.4).

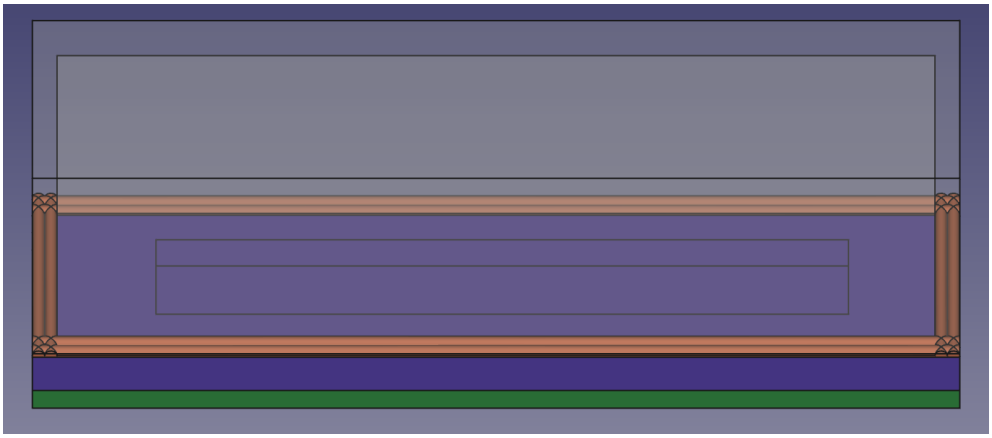

Figure 2.4: CAD designs of the isolation box. Hood partially transparent.

At the same time, the sides of the hood of the box would be cut from 2 cm foam and later assembled with the same PU glue. The box was designed with dimensions of 75 cm by 18 cm with 28 cm height, With to an internal volume of 71 cm by 14 cm by 20 cm. The wall thickness of 2 cm was chosen by calculating the thermal flux via conduction through the walls at a uniform thickness while under a temperature difference of $-60\,\mathrm{K}$ (25° C outside to −35° C inside). The following formula was used to make a conservative estimate of heat loss through the box via conduction:

$$q = -k \cdot \delta T \Rightarrow q = -0.032\,[\mathrm{W/(m \cdot K)}] \cdot (-60)/0.002\,[\mathrm{K/m}] = 96\,\mathrm{W/m^2}. \quad (2.1)$$

With the internal surface area being $(2 \cdot 0.71 \cdot 0.2 + 2 \cdot 0.14 \cdot 0.2 + 2 \cdot 0.71 \cdot 0.14)\,\mathrm{m}^2 = 0.5388\,\mathrm{m}^2$ one gets a heat loss of about 52 W maximum through conduction. To ensure good air tightness, the bottom piece of the box had a groove of 2 mm depth and 20mm width cut on the circumference of the top face in which a rubber window sill seal in the form of two side-by-side half circles was placed. The hood has a single half-circle seal placed at the bottom wall edge to create an interlocking seal between the hood and bottom piece that still allows for small cables to be passed through with relative ease and tightness. The hood was later shortened by 15 cm in height since the source system was placed outside of the controlled volume (see figure 2.5).

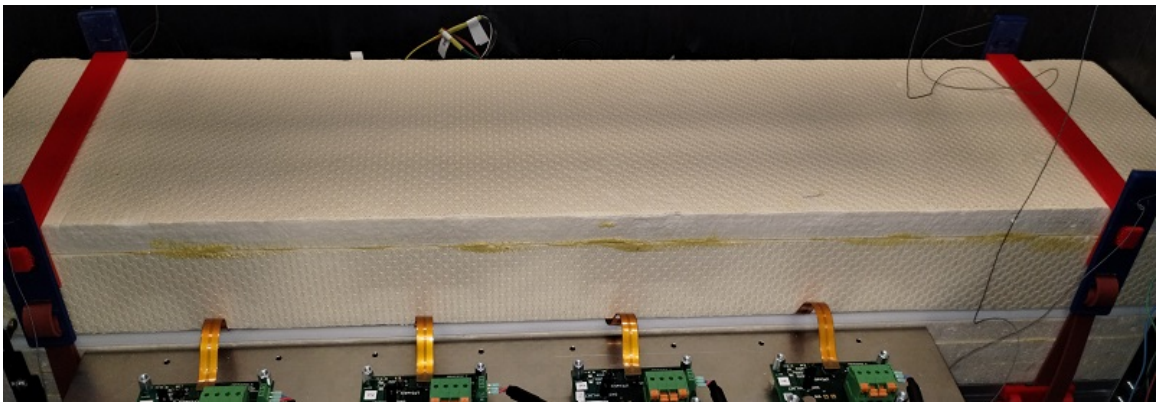

Figure 2.5: Finished isolation box in current setup.

Two layers of sealing lacquer were applied to the surface of the hat to eliminate dust from the crumbling of the isolation sheets.

2.6 Structural supports

The isolation box is supported by a frame made of a 25 mm by 25 mm extruded aluminum profile. The legs hold the box at a height of 15 cm above the surface of the lead enclosure. This allows for access to the various electrical and supply components and space to route the larger support lines, like the cooling fluid (12 mm diameter encapsulated in 6 cm diameter polyurethane isolation) through the bottom of the isolation. On the long side of the frame, two bent sheets of 2 mm aluminum are attached, to both provide side restriction to the isolation foam as

well as a mounting surface for the power and data adapters. The adapters sit level with the height of the modules inside the box to limit data/power-tail bending. On the front left leg, the lid switch is attached in such a way, that if the hat is in place, it is in a closed position. On the back legs, positioning plates are placed to ensure the correct placement of the lid (see figure 2.6).

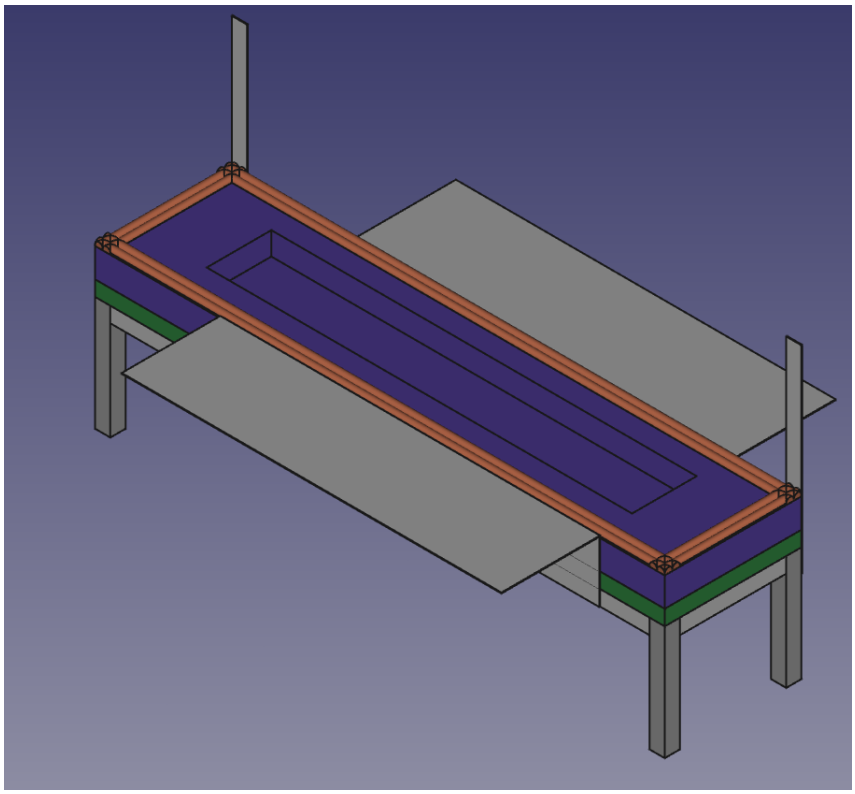

Figure 2.6: CAD designs of the structural supports.

2.7 Source system

2.7.1 Source

The radioactive source (74 MBq) for the test stand uses the isotope Sr^{90} to generate the energetic electrons necessary to trigger the pixels of the modules to test. This source generates two unique beta decay signatures with maximum energies of 546 keV for Sr^{90} to Y^{90} and 2.3 MeV for Y^{90} to Zr^{90}(stable). The Yttrium decay

has 2 negligible other beta decay channels which result in energetic Zr^{90} states that decay to the ground state via gamma rays. Therefore, the source can be assumed as a pure beta source for shielding purposes. The source is delivered as an 8 mm wide by 5 mm high cylinder with the Sr^{90} salts attached to a substrate as a 5.5 mm wide disc on the bottom of the source, sealed by a thin layer of aluminum foil. Due to this construction, the source radiates in a near semi-hemisphere unhindered (see figure 2.7 A).

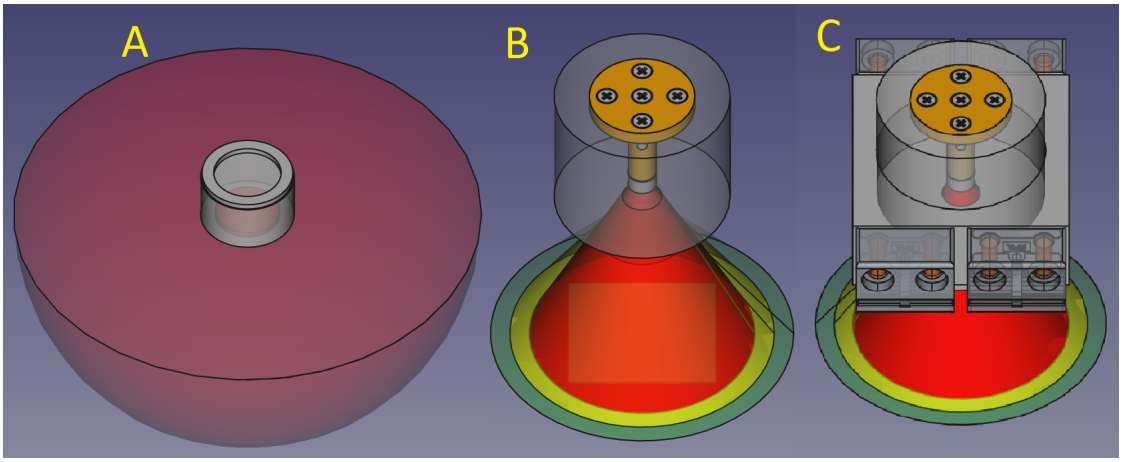

Figure 2.7: CAD designs of source A), source casing B), and source carrier C).

The casing and substrate of the source block nearly all beta radiation, which means it has to be carefully oriented in the mounting hardware in order to work. To better work with this source, a larger holding and focusing casing was built. This casing is a cylinder of aluminum with 50 mm width and 40 mm height. From the top, an 8.1 mm wide shaft is drilled 35 mm deep. This opening is for the insertion and housing of the source. From the bottom a 5 mm deep cut-off cone is machined into the cylinder with an opening angle of 51.2°, an upper opening of 6.5 mm width, and a bottom width of 11.3 mm. This creates a 0.8 mm wide ring against which the source rests, when inserted from the top, while keeping all of the active area of the source open to the to-be-illuminated region. The above numbers stem from the requirement to fully illuminate a 41 mm by 41 mm sized module with the source sitting at a height of 60 mm above the module sensor. This height was chosen, because the ITk testing team at Bonn University was operating a similar source (half of the activity) at this height at the time. To keep the source

securely in place, a 8 mm wide cylindrical insert with an inset mounting plate is screwed via four 10 mm M3 screws to the top of the mounting casing (see figure 2.7 B). The source mounting casing is then inserted in the movement system of the source source carrier as seen in figure 2.7 C.

2.7.2 Movement system

To use the source in an automatic fashion it needs to be able to be moved from a safe position, where all the radiation is blocked, to positions above the modules. This needs to be repeatable, reliable, and safe for the user of the test stand. Because of this, it was decided to use a 12 mm ball screw with a movement length of 600 mm and a lift height of 4 mm. Together with a stepper motor torque of 0.3 Nm, this system is capable of lifting $F = 2 \cdot \pi \cdot 0.3/0.004 = 471.24$ N, corresponding to 48 kg against gravity. Since it only slides a less than 1 kg load on a low friction horizontal sliding rail system, this is sufficient.

The rail system is built out of sliding rails from IGUS (drylin® W Einzelschiene WS) two 571 mm length and four sliding carriage pieces (drylin® W Gehäuselager WJ200UM-01) that hold up a custom-made carriage to both hold and further collimate the sources beam. The two rails, as well as the ball screw, are mounted on two bridge-like structures made of aluminum. The rails are attached at such height that the source inside the carrier will sit at a height of 60mm over the bottom of the aluminum bridges. The left bridge additionally contains the mounting points for the two end switches. One powers the source traffic light and the other the motor controller zero/end switch. The source garage blocks all beta radiation while in the zero position, and the end bearing housing for the ball screw is held by this left bridge. The right bridge holds the second bearing mount of the ball screw and the rails. There are no switches on the right end as the motor controller works on a step count system, that has been software-limited to a maximum of within 5 cm of this rail end. The motor is mounted inline to the ball screw via a custom 8 mm-to-5 mm aluminum adapter (see figure 2.8).

The structural mount of the motor was later changed from what is seen in the CAD drawing. The reason being that the source was found to be too strong for the chips' self-trigger/data output system, requiring the source to be further away

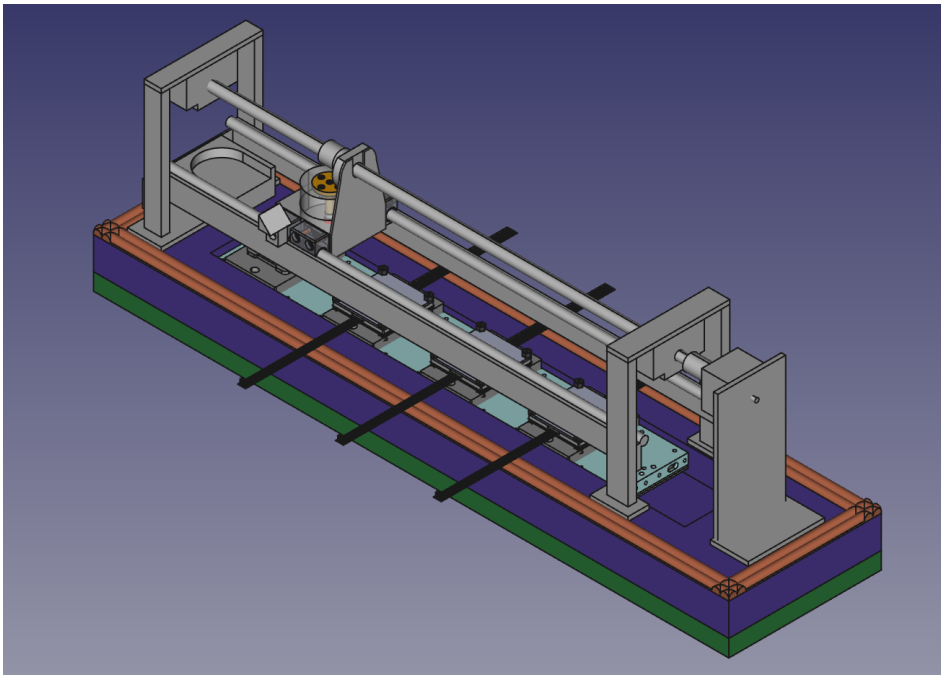

Figure 2.8: CAD design of the source movement system.

from the module, than the originally planned 60 mm. The new height is about 33 cm and required the mounting of the whole movement system under a 50 mm aluminum profile suspended inside the old setup 2 lead shielded box (see figure 4.8). This naturally meant the changes to the structural mount of the motor as well as additions to the tops of the bridges to allow for top mounting of the whole system.

2.8 Interlock system

The interlock system was developed by the Elektronikentwicklungslabor of the Department of Physics in Siegen. The interlock PC is a Windows 10 machine that runs 5 parallel programs to ensure/ allow the operation of the test stand. All of these programs were written and are maintained by the electronics laboratory. The requirements of these programs are provided by either the ATLAS Collaboration [19] or the users of the test stand. The following figure 2.9 shows the schematic design of the interlock system:

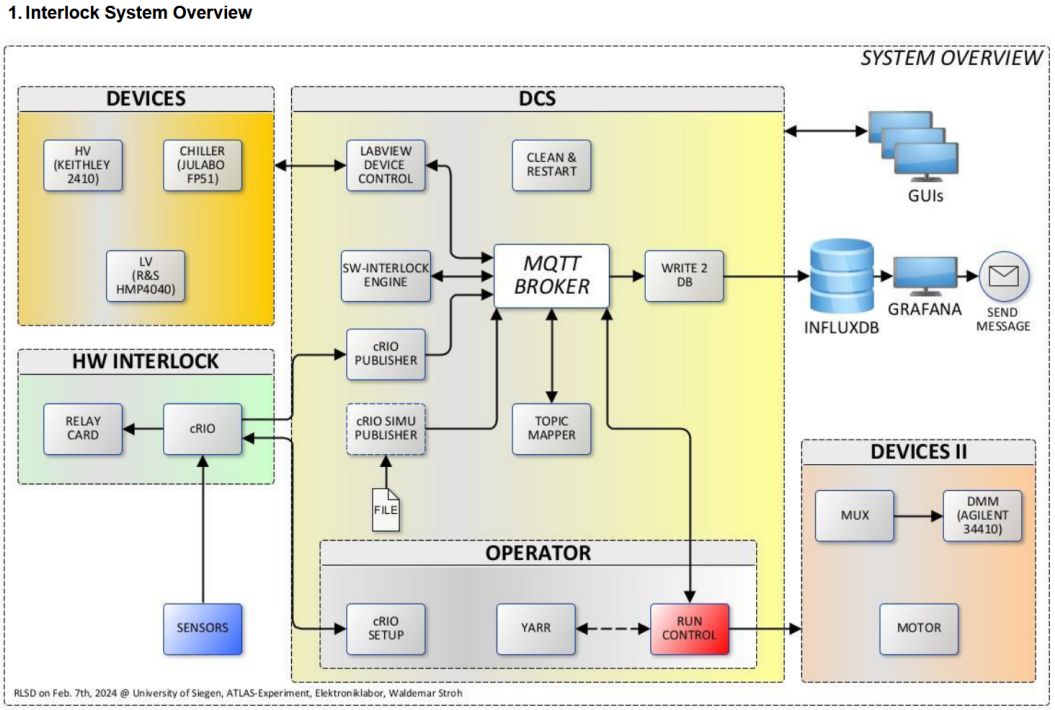

Figure 2.9: The interlock system schematics [23].

The following sections will describe details about the following points visible in the figure above:

1. Hardware interlock and sensors
2. Labview device control
3. Software interlock engine
4. cRio setup

The remaining parts will be described in the DCS section.

2.8.1 Hardware interlock and sensor system

The hardware interlock (HWI) is based on the commercially available cRIO system and the starting point for the code base was an implementation of the HWI system of the University of Glasgow. It was adapted by our electronics lab. The sensors read by the system are:

- 4 PT100 sensors reading the vacuum chuck temperatures
- an SHT85 (or equivalent) environment sensor
- an vacuum sensor
- an dry air pressure sensor
- up to four NTCs (one per quad pixel module)
- a lid switch

All of these sensors, excluding the PT100's, are collected on a custom PCB, where all connections are transferred via a sub-d connection to the custom power relay board. This board controls the power lines of LV and HV from the power supply units(PSU) to the module power adapter cards and is connected/controlled via another sub-d connection to the cRIO system. This allows the hardware interlock to shut down power forcefully if the necessary conditions are met. It is a safety feature to account for communication problems with the PSUs. The cRIO system itself is connected via ethernet to the MQTT server and isolated from outside control by design. Excluding the loading of the interlock configuration and exclusive control of the relay via MQTT topic to allow for serialized IV scans of 4 modules the relay has to be able to be remotely switched into a 1 to 1 connection instead of just 1 to many. The hardware interlock allows for setting of maximum environmental conditions on each of the mentioned sensors. Should they be exceeded, the module or all modules are shut off or are not allowed to be powered. In the following figure 2.10 the implemented HWI trigger settings can be seen:

2.8.2 Labview device control

This Labview program controls the communication with some of the peripheral devices that need to be accessed by multiple systems. It responds to certain MQTT topics to allow the control of the LV, HV and Chiller settings, and it monitors alarm states of the software and hardware interlock. It also periodically checks the function of the communication lines to the periphery and issues an alarm if they are broken. Should an alarm be triggered, the device control (DC) interface will automatically switch to its alarm tab flashing red and play an audible alarm signal. The MQTT communications are also checked against the program's

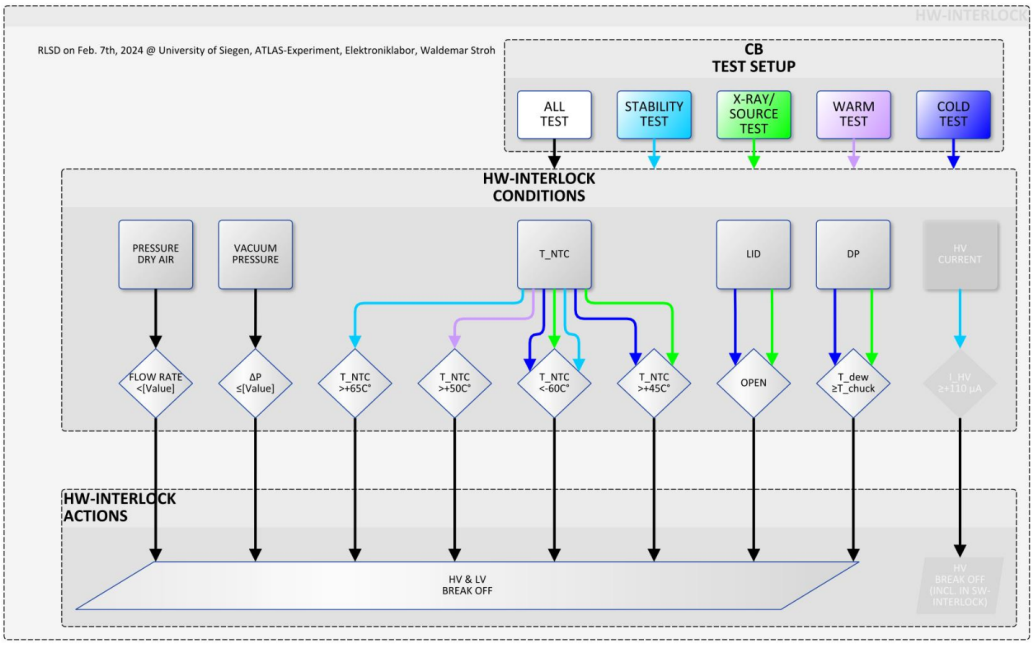

Figure 2.10: The HWI response schematics [23].

internal settings such that values outside of allowed parameter ranges are blocked from reaching the PSUs. The DC also checks and publishes (via MQTT) the set states of its controlled devices on a 3 s loop. The loop time is 3 s because of the response time of the LV PSU as it needs to publish 21 values: Four voltage setting and measurement, four current setting and measurement, four channel switch states and the main switch state. The following two figures 2.11,2.12 show the DC user interface:

2.8.3 Software interlock engine

The software interlock engine (SWINE) is a program to allow for softer responses to "alarm" conditions such as the dew point being too close to the vacuum chuck temperature. If in an active test state SWINE would issue a yellow alarm and raise the chiller temperature by 2° C to combat condensation. There are multitude responses programmed into SWINE, according to figure 2.13, sorted into 5 interlock states:

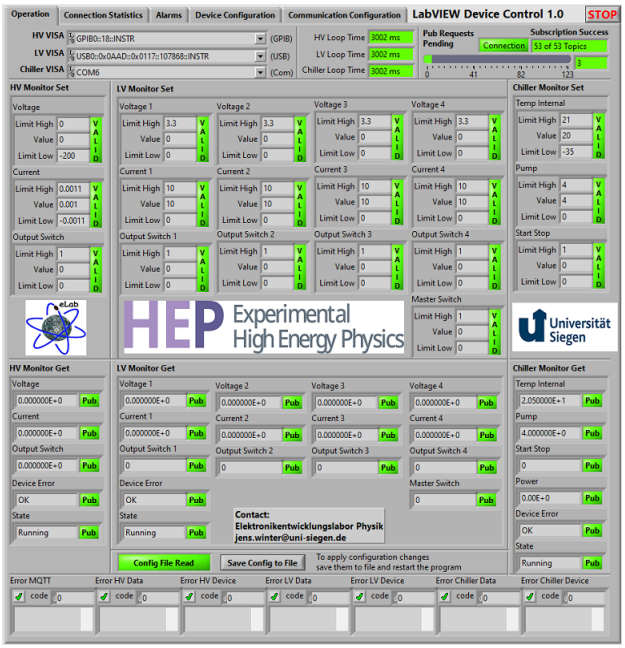

Figure 2.11: Device Control main screen.

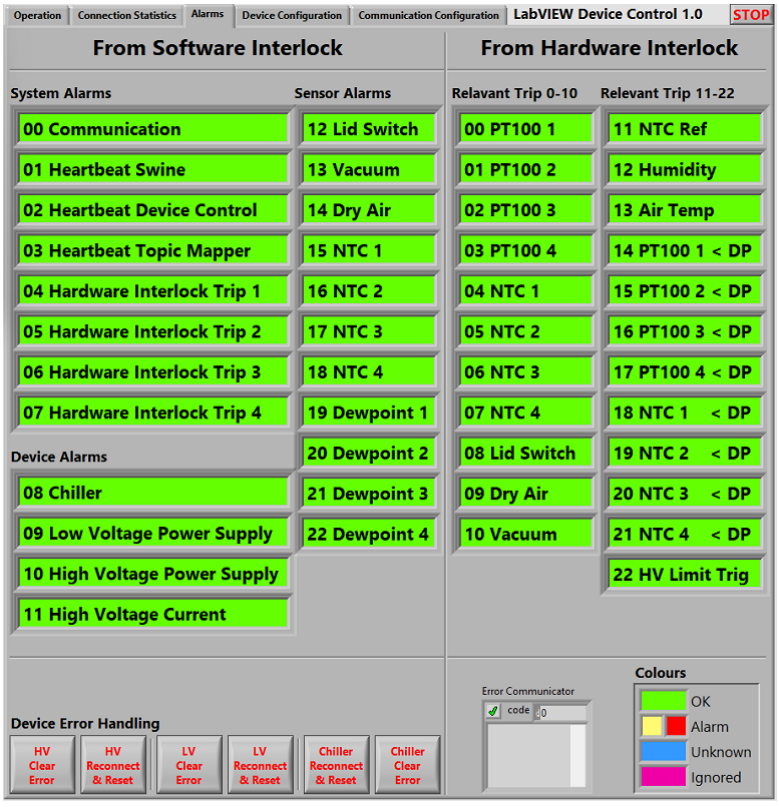

Figure 2.12: Device Control alarm screen.

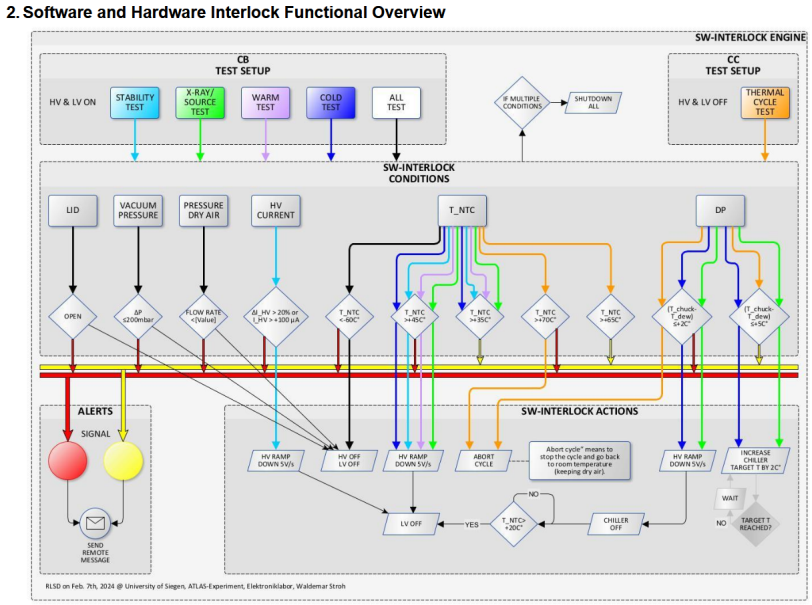

Figure 2.13: The SWINE response schematics [23].

1. idle: the system is active but no test response is loaded.
2. warm: the system is set to warm testing conditions.
3. cold: the system is set to cold testing conditions.
4. stab: the system is set to stability testing conditions.
5. source: the system is set to source testing conditions.

The software interlock is remotely controlled by the Run Control Software on the testing PC described in the chapter Run Control/DCS.

2.8.4 cRIO setup

The cRIO setup program allows the user to edit the cRIO configuration/trigger settings. This includes the addition and activation of one or multiple modules, activation/deactivation of trigger parameters, as well as changing of the trigger levels inside the parameters for up to four modules. Live data from the HWI sensors are displayed and logged for 60 s. This program cannot be interfaced or controlled remotely by design, so that no module can be powered while the testing

conditions are wrong. If the cRIO is triggered then a reset needs to be done via user input into this program. An exception to this rule was implemented that allows remote switching of the LV and HV relays to allow for serialised module testing as long as the module state in the HWI is ready. Figure 2.14 shows the user interface of the cRIO setup software.

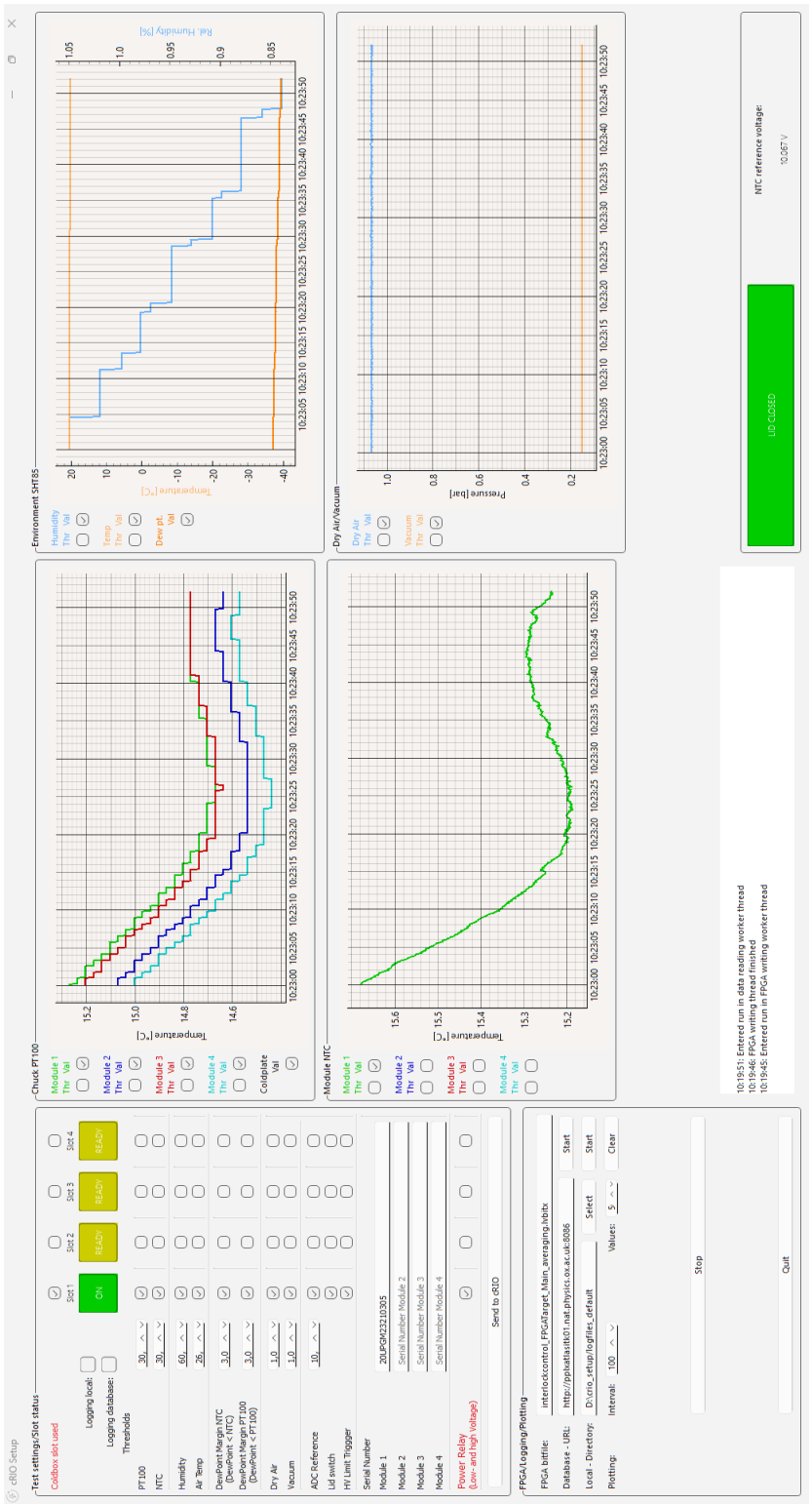

Figure 2.14: The cRIO setup interface.

3 Run control and DCS

The software development for run control (RC) and detector control system (DCS) went through several stages. Here the current state of the scripts will be described. A link to the code can be found in the Appendix.

3.1 The testing PC

The testing PC has an I9 processor at its core to handle the large amount of data that can be produced by running the ITk quad modules. The YARR (Yet Another Rapid Readout) card sits in one PCIe slot of the PC and allows for up to 16 chips to be connected in parallel. In addition to these connections, the PC is connected to the local internet network, needed for MQTT, and has connections via USB to the DMM and the source movement systems controller. The PC also hosts product and data partitions that are physically separated and mirrored onto two in-built hard drives via software RAID. Additionally, it is backed up to Siegen's computing cluster via a cronjob every night. On the software side, the PC houses the readout (YARR) and supporting software (MQC-tools), as well as the custom RC/DCS scripts for automated testing.

3.2 Communication module

The communication module MqttCourier is a Python module, adapted from the Python Paho MQTT client. The fist adaptation was done by the electronics lab and additions and fine tuning for the RC was done by me. It handles the MQTT communication of the main Python scripts. Its configuration file contains the necessary MQTT topics that provide data to and from the RC script. As soon as the class is initialized it writes all received messages of the to-be-read topics into a buffer dictionary. This can be accessed via the read topic command, which outputs the last received message on the asked for topic. This can cause issues with out-of-date data for the HV PSU. It was handled in the run state machine by checking if the output voltage matches the required values and if not restart/reenter the ramp state wait/check loop. This module is a parent of the state machine controller class which inherits some its functionality from the courier.

3.3 State machine controller

The Run module controls the state machines for the MQTT-controlled periphery ,via the device control software of the Interlock PC. It inherits from the MqttCourier and the three state machine classes for LV and HV PSUs and the chiller. Additionally to the inherited functions the Run class has five functions. Its initialization function sets the initial states. The second function checks the HWI via the courier and sets its attribute of active modules in the test stand. The last three functions are for switching the periphery state of the corresponding state machines. For the LV state machine, the states are simple, ON or OFF, since the testing power state of each channel is fixed at a standard value of 5.88 A and 3 V respectively. This causes the PSU to run in current supply mode as the module's internal resistance is too low to reach the 3 V requested voltage. The active module parameter limits which channels are sent the changes to their state. All other channels stay at the PSU power on parameters of 0 V, 0.01 A. There exists an ON CUSTOM state that lets the user set custom values for voltage and current settings. This is only used for debug purposes. For the HV state machine, the states are the same as for the LV, witch the exception that the ON and OFF commands correspond to ramping the voltage in 5 V intervals instead of setting it directly. The standard ON voltage for testing is -120 V with a current limit of $-100\,\mu$A current.

The environmental state machine for the control of the chiller has more states: START, IDLE, WARM, COLD, OFF. The START state is implemented for starting the chiller after system initialization. The switch-state function has an implemented check of the correct temperature state. If it is at the requested temperature it will not send a turn-on command. The initialization of the chiller sets it into IDLE and if room temperature fits within the IDLE temperature range and therefore causes no on-command to be sent. Should one desire to test in IDLE mode, as required for the stability test, this could cause problems as the temperature for turn on is only checked on mode switch command. The IDLE state sets the chiller set point to 21° C and the pump to full power. As mentioned before, if the average vacuum chuck temperature is within 3° C of the set point, no power-on command is sent. The WARM state has a set point of 14° C, which corresponds

to a running module temperature between just under 20° C for one module and just under 21° C for four powered modules. The COLD state has a set point of −24° C which corresponds to a running module temperature of between just under −15° C for one module and just under −14° C for four powered modules. The OFF state turns of the chiller controller and shuts down the chiller. There exists an ENV CUSTOM state that lets the user set custom values for set point and pump settings but this is only used for debug purposes.

3.4 Run and motor control

The run (run_Yarr) script contains the functionality for running the various sub-processes of the module quality control (MQC) software and the sub-processes for running the YARR scans and tunings. The MotorContol script is the communication link with the stepper motor controller (R256 controller from LinEngineering) for the source movement system. The contained command allows for re-zeroing the stage via the end switch and movement to the four module positions. The zero position functions as the safe/garage position for the source.

3.5 Periphery scripts for MQC-tools

The third party testing module for the MQC-tools needs direct access to some remote-controlled periphery devices. Direct access means running a script and then printing the answer as a number into the command-line interface (CLI) and terminating the script. This excludes the use of the MqttCourier custom modules, since they would need to stay active to gather the up-to-date messages and then be closed, severely slowing the response time. The solution to this problem is to run the mosquitosub CLI command on the necessary MQTT topic with only one received message as the reception limit. The received message is then printed into the CLI and the script is closed. To allow Python to run non-Python CLI code the module subprocess is used. If the script needs to send data to a device, the CLI command mosquitopub is used to send the data to the right MQTT topic. The scripts that use this method are needed for the control of the LV and HV PSUs as well as the module NTC data readout/data transfer.

There is a single other script that controls voltage measurements with the DMM. It requests a single measurement from the DMMs multiplexer card and needs the channel as an attribute. The script closes the selected channel, all other channels of the multiplexer are opened and then the measurement is taken. To ensure that all commands sent to the DMM are executed, the SCPI "*OPC?" command is sent and the script waits for an answer to that command before closing. The system paths to these scripts are documented in the MQC-tool configuration files together with the path to the YARR software. Each module position in the test stand has a dedicated configuration file as the MQC software currently only supports single module testing.

3.6 Module QC-tools

The module QC-tools (MQC-tools) are a collection of three third party Python modules developed by the ITk pixel testing community. They are designed to handle the database connection, "external" testing of the pixel modules, and analysis of the results. They are named MQC-database-tools, MQC-tools, and MQC-analysis-tools, according to their functions. The database tools are used in to download the YARR module configurations from the production database. This is done during the closing steps of the module assembly or initial step of module testing. The configuration files are saved and the working copy is then updated through the testing tools.

The testing tools contain the "external" tests for the module. This means that for these tests some data from an external device is necessary to analyse module functionality.

These tests are in order of QC procedure: High voltage IV-measure, ADC-calibration, analog-readback, SLDO, VCAL-calibration, injection-capacitance, LP-mode, overvoltage-protection, undershunt-protection, data-transmission. Details of these tests are found in the following sub-sections. The analysis tools contain the scripts necessary to analyse MQC tests and update the module configurations according to the results.

3.6.1 IV-MEASURE

This script measures the pixel sensor by setting the HV PSU to predefined values and measuring the leakage current. The plotted result (see figure 3.1) shows the sensor's diode curve in the voltage range from 0 to −200 V. From this, depletion and breakdown voltages are calculated. The module NTC temperature is taken into account to be able to compare the data to the IV curve measured for the bare module. This is done to see if assembly or wire bonding damaged the sensor.

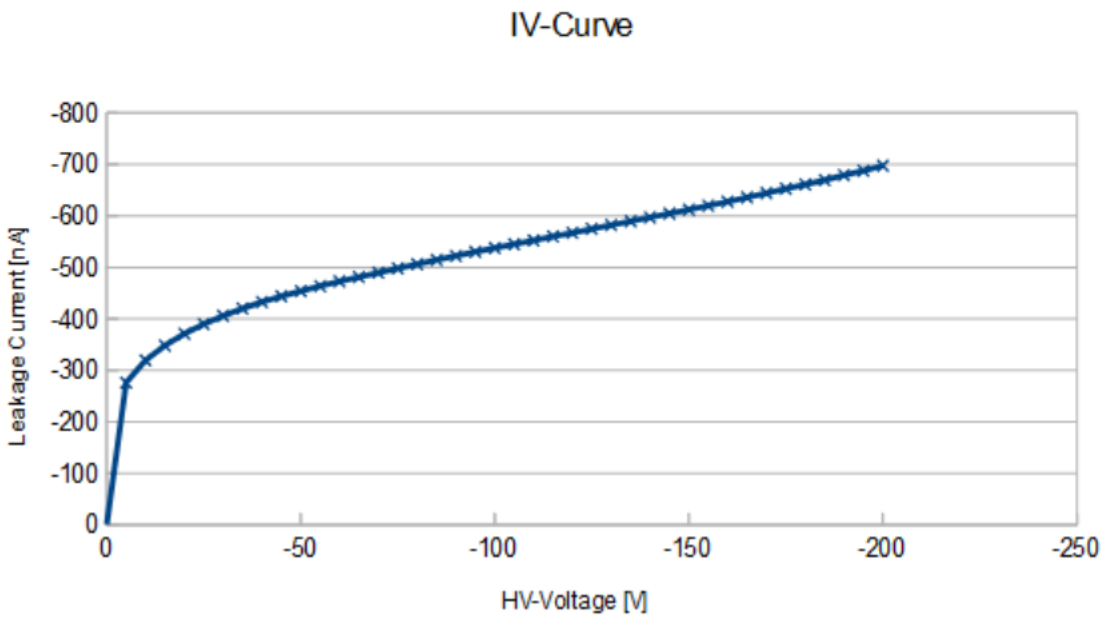

Figure 3.1: Post assembly IV-curve for module 20UPGM22110464.(25V depletion, no breakdown observed)

3.6.2 ADC-CALIBRATION

The script calibrates the chip's internal analog-digital converters via referenced readout through the Vmux multiplexer (chip internal voltage multiplexer) with a high-precision digital multimeter.

The ADC parameters are measured at fifteen fixed points of the DAC for all four chips through one output line on the module (shared Vmux). These data points are the fitted with a linear regression to calculate the ADC slope, offset,

linearity. The script additionally checks the chips ground potential in comparison to the module ground.

The corresponding analysis script calculates the linear output equation (see figures 3.2 and 3.3) for the chip ADC/DAC system and then the update-chip-config script is used to write the data to the chip configuration files.

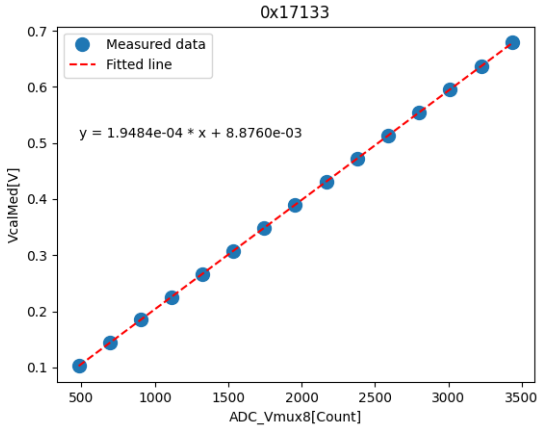

Figure 3.2: ADC data and fit for chip 0x17133.

ADC_CALIBRATION for 0x17133

Parameter	Analysis result	QC criteria	Pass
ADC_CALIBRATION_SLOPE	0.195	[0.15, 0.224]	True
ADC_CALIBRATION_OFFSET	9.0	[-9, 31]	True
ADC_CALIBRATION_LINEARITY	0.25	[0.0, 4.0]	True
ADC_ANAGND30_MEAN	0.086	[0.015, 0.023]	False
ADC_ANAGND30_STD	0.0	-	-

Figure 3.3: ADC parameters for chip 0x17133.

3.6.3 ANALOG-READBACK

This script performs a general test of the chip's internal sensors and registers. For example, the data output is used to adjust the VDDA/VDDD trim, to ensure that the internal power lines of the chip run at the required 1.2 V. Various registers are

checked for correct responses. Iref (internal current reference), in particular, needs to be close to 4 μA, as this would confirm the correct wire-bond placement for an outer barrel module. Additionally, the internal temperature sensors are checked against external measurements. The following figure 3.4 shows the results for a chip in the analog-readback QC test.

ANALOG_READBACK for 0x17133

Parameter	Analysis result	QC criteria	Pass
Iref	3.8e-06	[3.6e-06, 4.2e-06]	True
GADC	0.839	[0.703, 0.924]	True
VcalDac	0.843	[0.668, 0.987]	True
VrefCore	0.449	[0.435, 0.49]	True
VrefOVP	1.943	[1.857, 2.152]	True
ChipNTC_vs_ExtExt	0.5	-	-
AR_VDDA_VS_TRIM_2	1.07	[0.0, 1.2]	True
AR_VDDA_VS_TRIM_13	1.266	[1.2, 2.0]	True
AR_VDDD_VS_TRIM_2	1.067	[0.0, 1.2]	True
AR_VDDD_VS_TRIM_13	1.261	[1.2, 2.0]	True
AR_ROSC_SLOPE	[756.6 ... 1523.25]	-	-
AR_ROSC_OFFSET	[-439.24 ... -1025.14	-	-
AR_ROSC_MAX_RESIDUAL	[1.53 ... 1.09]	-	-

Figure 3.4: Analog Readback summary for chip 0x17133.

3.6.4 SLDO

This script tests the chip's shunt-LDO system in an overcurrent situation. The overcurrent condition can occur if one of the chips breaks while the module is part of a serial-powered chain of modules. Therefore, the other chips have to handle 33% extra current going through their power system. To simulate this situation, the module is powered at a maximum of 9.488 A and then decreased in 200 mA steps to chart the chip's responses.

3.6.5 VCAL-CALIBRATION

This script measures and calibrates the chip's electron chopping circuit. This circuit generated discrete packages of electrons to be used in the pixels analog detection system as a replacement for a real signal from the sensor. The calibration allows for the association of a number of electrons to the internal VCAL unit (see figure 3.5).

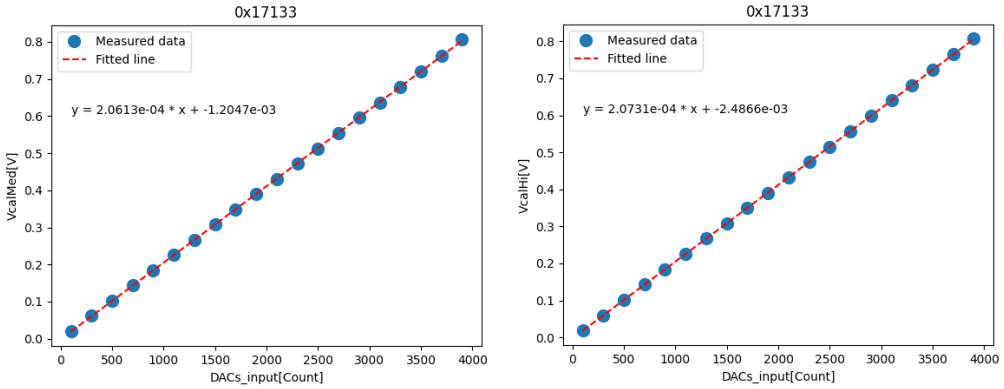

Figure 3.5: VCAL MED (left) and VCAL HIGH (right) fit for chip 0x17133.

The circuit signal is generated via a differential of two voltages named VcalMed and VcalHigh. It is necessary to check that these voltages behave linear and update the configuration with the linear parameters, since the chip tuning is in VCAL units and the target is a given number of electrons. The calculated formula is again saved into the chip configuration files after the analysis is done. Figure 3.6 shows the calibration results of a chip.

3.6.6 INJECTION-CAPACITANCE

This script calculates the capacitance (see figure 3.7) of the internal injection capacitor, which takes and stores the VCAL units after the chopping circuit for later use. The data is saved to the chip configuration files after the analysis.

VCAL_CALIBRATION for 0x17133

Parameter	Analysis result	QC criteria	Pass
VCAL_MED_SLOPE	0.21	[0.16, 0.24]	True
VCAL_MED_OFFSET	-1.0	[-23, 17]	True
VCAL_MED_LINEARITY	1.1	[0.0, 4.0]	True
VCAL_MED_LINEARITY_SMALL_RANGE	0.63	-	-
VCAL_HIGH_SLOPE	0.21	[0.16, 0.24]	True
VCAL_HIGH_OFFSET	-2.0	[-23, 17]	True
VCAL_HIGH_LINEARITY	0.42	[0.0, 4.0]	True
VCAL_HIGH_LINEARITY_SMALL_RANGE	0.42	-	-
VCAL_HIGH_SLOPE_SMALL_RANGE_RATIO	0.5	[0.49, 0.51]	True
VCAL_MED_SLOPE_SMALL_RANGE_RATIO	0.5	[0.49, 0.51]	True

Figure 3.6: VCAL Calibration summary for chip 0x17133.

INJECTION_CAPACITANCE for 0x17133

Parameter	Analysis result	QC criteria	Pass
INJ_CAPACITANCE	7.59	[6.74, 9.0]	True

Figure 3.7: INJECTION-CAPACITANCE summary for chip 0x17133.

3.6.7 LP-MODE

This script tests the functionality of the chip's low power (LP) mode. The YARR card is set to output a certain frequency to activate the LP mode in the chip. This increases the internal resistance, allowing for the chip's working point to be achieved at lower current inputs. The analysis checks for the generated voltage at LP current to be within required levels ($1.6 - 1.8\,\mathrm{V}$ at $2.1\,\mathrm{A}$), as well as that the generation of internal voltages is still functional at $1.2\,\mathrm{V}$. An lpm_digitalscan (see YARR digitalscan 3.7.1) is also run to check the digital pixel functionality in LP mode.

3.6.8 OVERVOLTAGE and UNDERSHUNT-PROTECTION

These scripts check the functionality of the overvoltage and under-shunt protections.

3.6.9 DATA-TRANSMISSION

This script is the MQC equivalent of the YARR eye-diagram and checks for a functional sync of the aurora communication protocol. The RD53 chip runs on an phase locked loop clock of 40 MHz that is internally multiplied to 160 MHz. This 40 MHz signal is supplied to the chip via the command input line of the chip during down time in the aurora communication protocol. The protocol nominal message is a sync pattern that the internal clock uses to sync to the readout. If that is correctly received the chips responds by repeating the pattern on the chips output with a chip inherent delay that need to be checked and the readout setting adjusted to allow for stable communications with the chip.

3.7 YARR

YARR is a dedicated readout software for the RD53 chips. It is able to control various hardware cards connecting to the RD53 modules. In Siegen, YARR runs a Trenz Electronics TEF-1001 R2 microcontroller card with an Ohio-designed adapter card. The software is based on C and controls all scans done on the RD53 chips. YARR commands are run in the standard command-line interface. YARR

supports a number of scans described in the following sub-chapters with plotted results from a module tested with the Siegen test stand.

3.7.1 Digital scan

The YARR digital scan simulates a hit in the RD53 chip by setting the digital hit register to a time-over-threshold (TOT) setting of 7(4 bits) and then reading the pixel matrix. One hundred iterations are recorded with the result displayed as a 2D colored map of the pixel matrix (see figure 3.8).

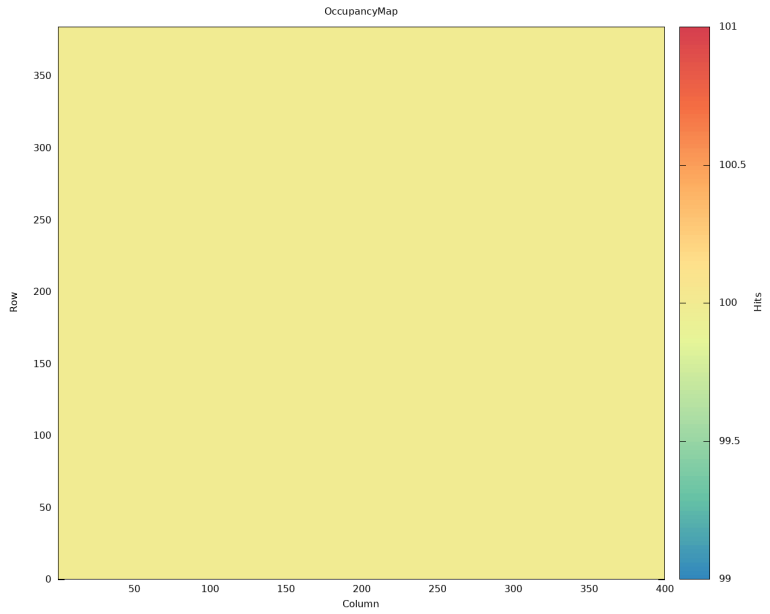

Figure 3.8: Digital scan pixel matrix plot for chip 0x17133.

The expected result is 100 registered hits on every pixel. Non-functional pixels (0 hits) are automatically added to the disable mask and will no longer be readout by other scans, unless forced.

3.7.2 Analog scan

The YARR analog scan mirrors the digital scan in the analog electronics of the chip. Electron charges far above the hit threshold are injected into an analog pixel to simulate a charged particle hit in the sensor. As the pixels analog circuits are

used, the results are expected to be more noisy in the 2D map (see figure 3.9) with hit results between 95 and 100 being acceptable before tuning of the chip.

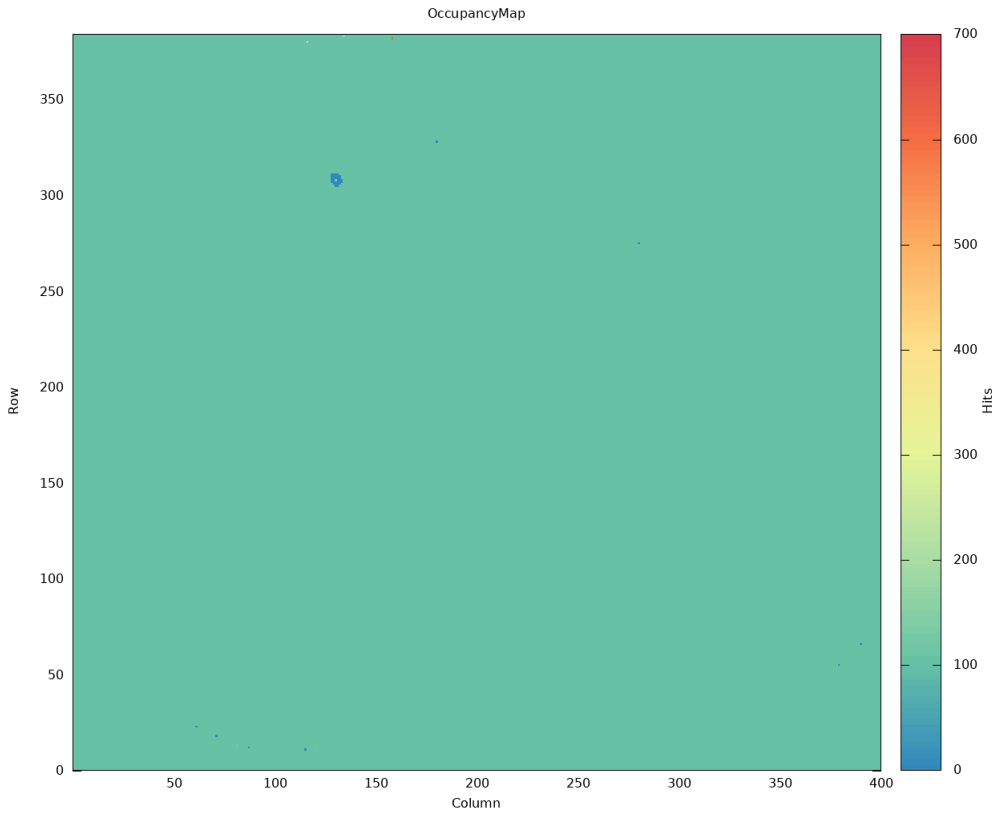

Figure 3.9: Analog scan pixel matrix plot for chip 0x17133.

In figure 3.9 a typical analog result is visible with some pixel on the chip edge receiving multiple hits due to the gab recovery causing bad contrast. Additionally visible is a cluster of dead pixels in the upper right quadrant of the chip and some single dead pixels in the bottom half of the chip. The later analyses of the scans adds these to the chip characterisation as analog broken pixels.

3.7.3 Threshold scan

The threshold scan maps the pixel response to injected charge values by running a series of analog scans at different injection values. The threshold is defined as the value of charge where the pixel triggers 50% of the time. The chip's response

is very different between an untuned(only global response) and a tuned chip, as visible in the figures 3.10 and 3.11 below.

The suffix of "hr" and "hd" mean high range and high definition, causing the scan to either be done from very low to very high values of VCAL with a wide step size or a smaller range around the working point of the chips at a small step size in VCAL.

3.7.4 Tuning the global/pixel threshold

These YARR scripts allow for adjusting the global pixel matrix amplifiers and the local pixel amplifiers.

The global scan adjusts the general response of the pixel matrix to the set target number of electrons. Typically this is first 2000 electrons and then retuned to 1500 electrons. Two steps are necessary, since some pixels have issues when directly tuned to 1500 electrons from their starting value of around 3500 electrons.

The pixel scan adjusts the local pixel amplifiers via the TDAC setting. The TDAC setting a matrix with a 4 bit value corresponding to each pixel of the chip. The default setting of this matrix is 7 and 8 alternating between pixels. The pixel scan goes through seven TDAC tuning steps of sizes (4,2,1,1,1,1,1) with the first four being necessary to achieve the full range of possible setting and the last three being fine-tuning and checking response smoothness. The purpose of the pixel scan is to smooth the response of the pixel matrix as much as possible around the set tuning point.

3.7.5 Noise scan

The YARR noise scan just reads out the pixel matrix with a random pattern of triggers for about 11 million triggers. This takes approximately 90 seconds. Pixels above a certain number of hits are marked as noisy and removed from the active pixel matrix in the configuration file. Conditions in the test setup are such that no pixel should record a hit, barring ambient radiation, unless they are noisy.

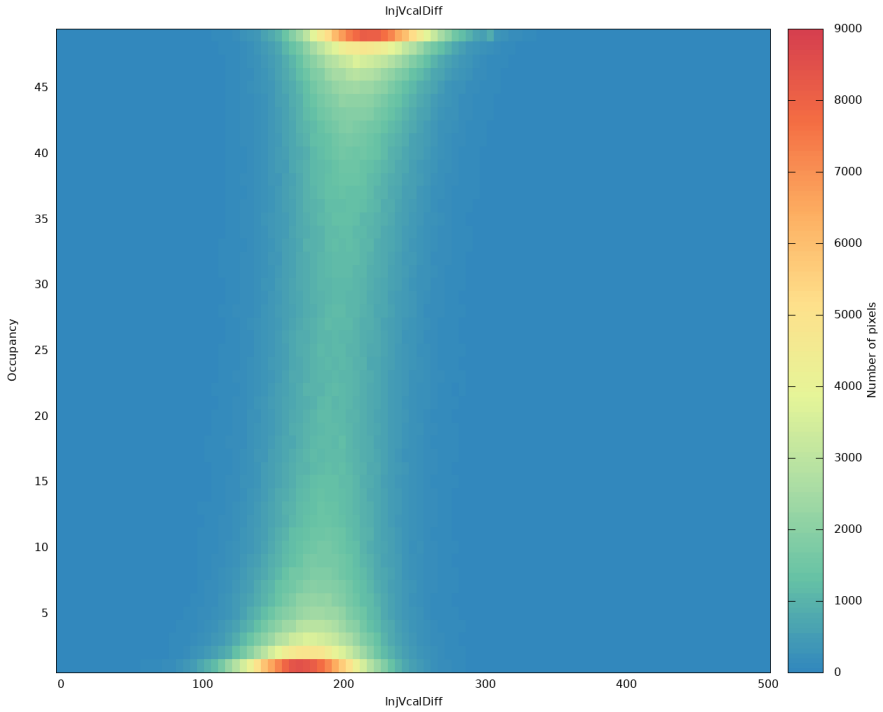

Figure 3.10: 3D pixel response plot for chip 0x17133, global tuned to 2000 e^-.

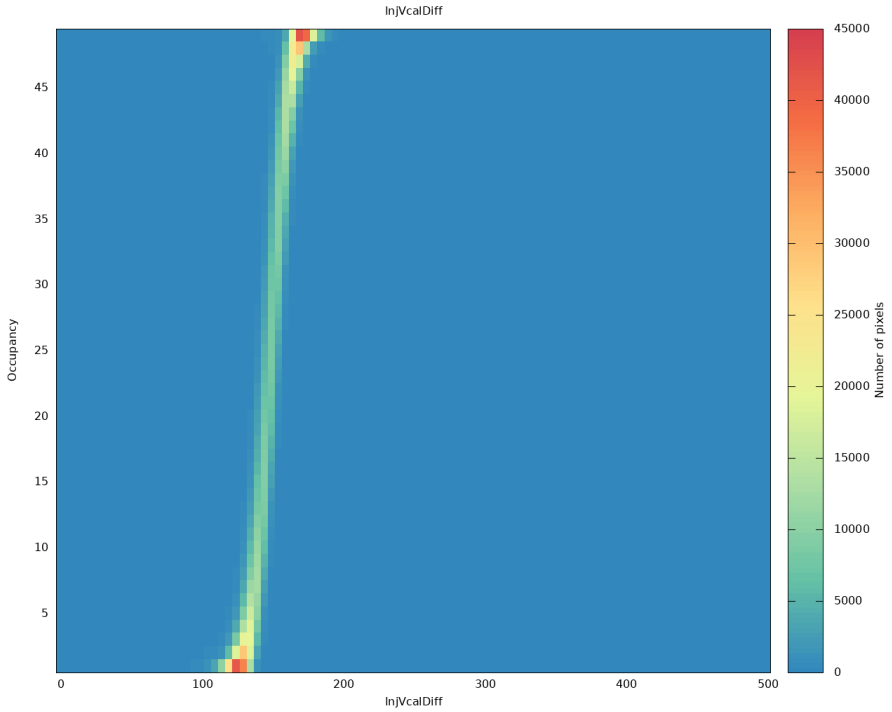

Figure 3.11: 3D pixel response plot for chip 0x17133, fully tuned to 1500 e^-.

3.7.6 Disconnected bump scan

The disconnected bump scan checks for disconnect bumps from the side of the chip without requiring a source to illuminate the sensor pixels.

3.7.7 Merged bump scan

The merged bump scan checks for merged bump bonds.

3.7.8 Source scan

The source scan starts by setting the chips into self-trigger mode. This means that whenever a pixel is hit, the corresponding chip self-generates a readout trigger and sends the data out to be read. Therefore, the readout rate is limited by the data-out capability of the chips. For the outer barrel modules this corresponds to one line of 1.28 GBit/s per chip, currently, while for future modules $\frac{1}{2}$ line per chip (two chips sharing lines) or $\frac{1}{4}$ line per chip (four chips data sharing) are foreseen. This imposes a soft trigger limit on the self-trigger since the output buffer of the chip would overflow and cause communication failures, when the trigger rate is too high. The soft limit for modules with four output lines is measured to be around 62.5 kHz, as the closest we could place the Sr^{90} source without occasional communication failures creates around 250000 hits per second scan time. Therefore, and owning to the Flex absorption properties, the source scan has to last 30 min to achieve the required 10 hits per pixel. See figures 3.12 and 3.13 for examples.

The main problem areas are underneath the power and data connectors which, add $2 - 4$ mm (power connector and pins) or 1 mm (the data connector) of low Z material. The maximum penetration depth of the source is in the range of 5 mm aluminum with most of the source spectrum being far less powerful than this.

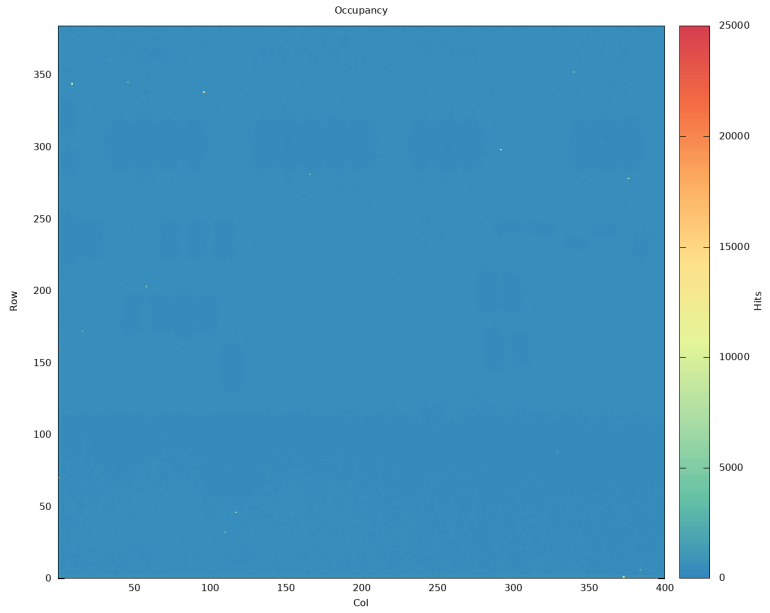

Figure 3.12: Source scan occupancy after 30 min irradiation for chip 0x178d8 as generated by YARR.

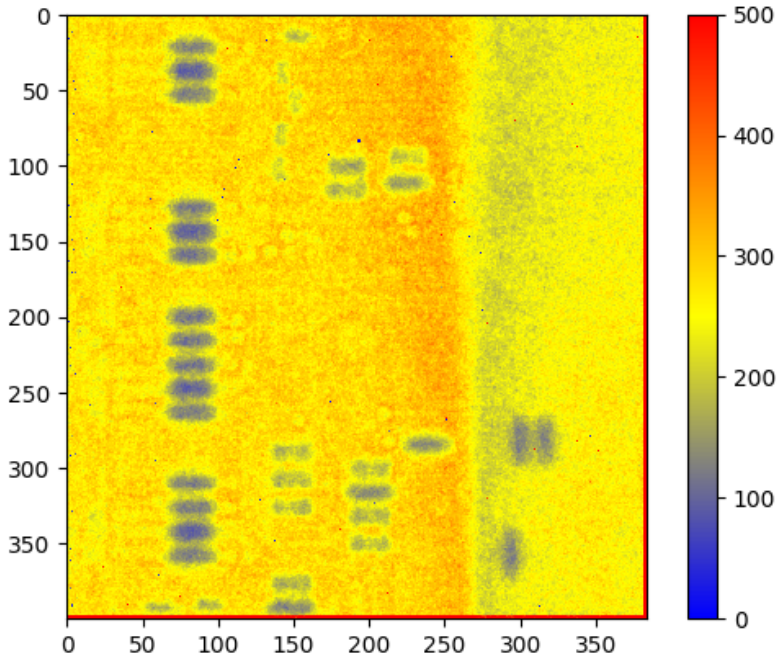

Figure 3.13: Same source scan occupancy for 30 min irradiation for chip 0x178d8 with custom z-scale (max. 500) and rotated to match real chip orientation in the setup.

3.8 Run control

The main run control / DCS script is called Menu.py. It is a custom command line-based script that allows the user to navigate the test stand's functionality via different interactive menus in the terminal. The menu functionality is achieved via the module CLICK which allows for queries to be sent to the terminal and only continue the script, if a valid input by the user is given. When activated, the script first initializes a courier object from the MqttCourier class. Ten seconds later, the courier object is handed over to a run object initialized from the Run class. The waiting time is implemented to allow the courier time to fill its message dictionary with MQTT messages. The slowest of the messages are published on a 3s cycle time. then, the run object generates a list of active modules (published by cRIO) that is saved in a variable (Mod) for later use. After this Mod is now used to update the active module's YARR configuration files to match their positions inside the test stand. When this is completed the menu loop flag is set to true.
The following main menu options are described in the next sub-sections: ENV, LV, HV, SOURCE, STATE, TEST, RELOAD, EXIT.

3.8.1 ENV, LV and HV-menus

The environment menu ENV allows for manual control of the environment state and the chiller via the state machine controller. This menu lists the options for the chiller state machine described in the previous section on the state machine controller. The same applies for the LV and HV menus.

3.8.2 SOURCE-menu

The SOURCE sub-menu allows for the manual movement of the source via the MotorControl functions. Options, as previously mentioned, are: SAFE, 1, 2, 3, 4, with SAVE being the zero / garage position of the source and the numbers correspond to positions directly over the top of the module with the selected number.

3.8.3 STATE-menu

The STATE sub-menu allows for manual control of the SWINE states with the options mentioned in its paragraph.

3.8.4 TEST-menu

The TEST sub-menu holds the options for manual and automated testing. These options are EYE, DIGI, ANA, and THR that run the YARR scans eye diagram, std_digitalscan, std_analogsscan, and std_thresholdscan. The scans are executed in series for all active modules. The options QC and FULL_QC run the QC procedure either in warm or cold (QC), or both (Full_QC). The QC procedure is described in section 3.8.7. All active modules are run through the procedure in series. The option PFA runs the Pixel Failure Analyses part of the QC procedure. Finally, the option STAB runs the stability test routine.

3.8.5 RELOAD

The RELOAD sub-menu updates the Mod variable with the current active modules and updates their configuration files to their respective test stand positions.

3.8.6 EXIT

The main menu EXIT causes the periphery to be set back into an idle/off mode and returns a false to break the main menu "while" loop causing the main script to finish. The periphery exit happens by first setting the HV state to OFF, followed by setting the LV state to OFF. Then the ENV state returns to IDLE, heating the chiller to 21° C, and after that the state is set to OFF, turning the chiller PID controller off. Finally, the MotorController receives a signal to move the source to the SAFE position, ensuring that the radioactive source is stowed behind the shielding.

3.8.7 QC procedure

This section describes the actions the test stand's systems have to go through to complete one electric test cycle/stage. Each module is tested twice. One time

warm at an active module temperature of 20° C, and one time cold at −15° C. The testing procedure is as follows.
Establishing initial testing conditions:

- Set LV to OFF
- Set HV to OFF
- Set HWI active module to the required channel
- Set ENV state to warm or cold
- Wait for 60 s after ENV conditions are met
- Set LV to ON
- Set HV to ON
- Set SWINE to WARM or COLD

Beginning the QC sequence with MQC-tools tests:

- Run MQC IV-MEASURE
- Run YARR EYEDIAGRAM (ensuring good connection)
- Run ADC-CALIBRATION
- Run ANALOG-READBACK
- Run SLDO
- Run VCAL-CALIBRATION
- Run INJECTION-CAPACITANCE
- Run LP-MODE
- Run OVERVOLTAGE-PROTECTION (not required anymore)
- Run UNDERSHUNT-PROTECTION (not required anymore)
- Run DATA-TRANSMISSION

These tests ensure the minimal functionality of the module by probing the chips and updating the chip's configuration files. After these initial testing conditions, the module is ready for the more complex YARR scans starting with the Minimum Health Test (MHT) Block:

- Run digital scan
- Run analog scan
- Run threshold scan (high range)
- Run TOT scan (6000 e^-)

This series of scans determines the functionality of the module. Following the MHT is the TUNING (TUN) procedure which calibrates the chips to the nominal testing/detector threshold settings. To do so the following block of YARR scans is run:

- Run tune global threshold (target 2000 e^-)
- Run threshold scan (high range)
- Run tune pixel threshold (target 2000 e^-)
- Run retune global threshold (target 1500 e^-)
- Run retune pixel threshold (target 1500 e^-)
- Run threshold scan (high definition)
- Run TOT scan (6000 e^-)

The last step of the QC procedure is the Pixel Failure Analysis. This series of scans tests the functionality of the hybrid pixels. The following YARR scans are included in the PFA block:

- Run digital scan (reset mask parameters to default)
- Run analog scan
- Run threshold scan (high range)
- Run noise scan
- Run disconnected bump bond scan
- Run merged bump bond scan
- Set HV to OFF
- Run retune pixel threshold (target 1500 e^-)

- Run threshold scan (zerobias)
- Set HV to ON
- Run retune pixel threshold (target 1500 e^-)
- Set SWINE to SOURCE
- Set source motor to module position
- Run self-trigger scan (30min)
- Set source motor to the SAFE position

The first three scans check for broken pixels in the digital, analog, and tuning layers of the chips. The noise disconnected and merged bump scans are all different checks on the quality of the bump bonds that can be done from the chip's side. Finally, a 30-minute source scans with the Sr^{90} source over the module checks on the pixel functionality from the sensor side of the module. Before the source scan is executed the SWINE is set to the source scan parameters, the source is moved into position over the module and afterwards returned into the safe/garage position. The QC procedure ends with the SWINE being reset to IDLE conditions. Not specifically mentioned is that for every scan/test, there is a check in place after the scan to ensure that testing conditions stay within expected parameters. If this is not the case the script skips the following scans and continues testing the next module.

4 Commissioning: An assembly report

4.1 Test stand enclosure

While the parts described in chapter 2 were in production and assembly, the decision of where to install the new test stand was taken. Due to the necessity of using a strong Sr^{90} source, the whole setup must be shielded. This led to the decision to reuse the shielding setup of the first ATLAS module production in Siegen.

The setup has an internal volume of 79 cm width, 54 cm depth, and 72 cm height. All sides, other than the top, are lined with 5 mm thick lead sheets. This amount of shielding was necessary, as the old setup used an Am^{241} gamma source to illuminate the inner pixel detector (ID) modules during testing. The setup contained a Peltier cooler connected to the holding block capable of mounting two ID modules and a movement system to move the Am source from the shielded garage into either position over the two modules. Everything other than the lead shielding was removed from the shielded enclosure. This included breaking the positioning strips for the cooling block and the source garage from the lead sheets as they were glued. The Peltier cooler was taken out of the box and put into storage. The old source movement setup was disassembled and, except for the aluminum profile holding the system, put into storage. This aluminum profile was later used to mount the new source system. Lastly, the shielding plate underneath the Peltier cooler exhaust was removed, as the space was necessary for future cabling and cooling pass-through. This was possible as the resulting hole would be underneath the new cooling plate and would not compromise shielding for the new Sr^{90} source.

4.2 Cooling circuit

After the test system parts were manufactured, they were moved into the enclosure and needed to be connected to the support infrastructure. This sub-section focuses on the cooling circuit as it was the most labor intensive. The new cooling plate has in/outlets for the cooling liquid on the left side of the isolation box pointing downwards.

In the first iteration of the cooling circuit, the cooling plate connectors were connected to 12 mm Festo tubing going out from the bottom of the isolation box. They then pass diagonally through the enclosure hole and follow beneath the enclosure floor to the chiller on the right (see figure 4.1).

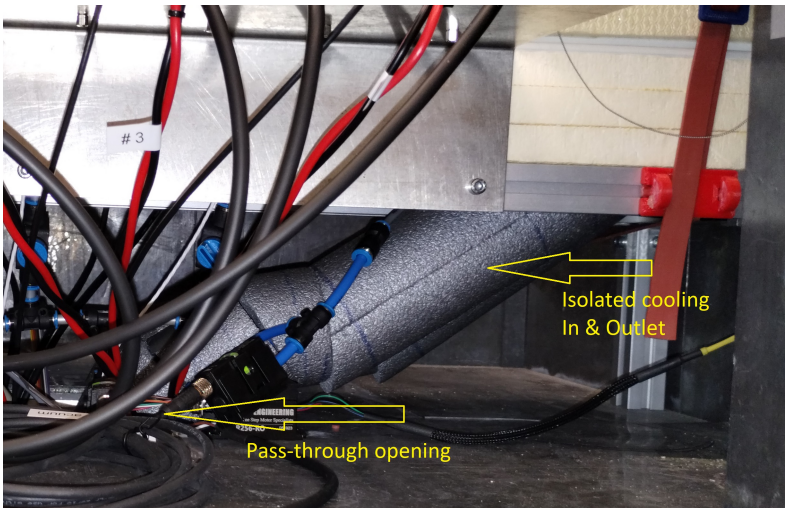

Figure 4.1: Enclosure cooling routing.

Two custom thread adapters connect to the chiller's thermal bath via 90° Festo adapters to the tubing. This tubing was then covered in a 6 cm diameter PU insulating tube. This insulation had to be cut into custom pieces to follow the tubing as it had bend ability properties similar to a pool noodle. After the first test it was discovered that the tubing was slack and parts not covered by the insulation anymore. Prolonged contact with the 80-ethanol-20-water mixture, that is used for cooling, causes the Festo tubing to swell/expand slightly. This increase in size is about 1–2% which corresponds to about 2 cm over the 2 m length of tubing and was visible, as the previously flush pieces of insulation were pushed apart. The problem was fixed by moving the chiller away to pull the tubing tight and extra insulation pieces were added to cover the full tubing again.

The second iteration of the circuit happened because the lab was rearranged and it was decided to use the dead space the enclosure door generates to house the chiller. As this space is to the left of the enclosure, the insulation for the cooling tubing needed to be removed and reassembled to fit the new path. During

this operation, it was discovered that the tubing not only lengthened due to the exposure to the cooling mixture, but it also increased in diameter. The increase in diameter made disconnection hard and reconnection impossible without leaks. Therefore, the cooling tubing needed to be replaced.

The third iteration was necessary because of a fix a to a problem observed in the dry-air system. The cooling plate was designed to cool the dry air as well as the modules, and observation showed that the air temperature in the box stayed constant near room temperature. To aid the dry-air cooling, a pre-cooler was designed, cooled by the returning cooling liquid from the test stand. To insert the pre-cooler, the return line had to be shortened by 15 cm. The tests with pre-cooler where problematic as the design leaked cooling liquid and did not aid the problem measurably. It was then decided that the air temperature is not relevant any more as the new humidity sensors and air dryer allowed for more precise measurement of the the relative humidity and delivery of more dry air to the system to allow for quick cold testing. When the pre-cooler idea failed the return line was replaced as it was too short to reach the chiller (see figure 4.2).

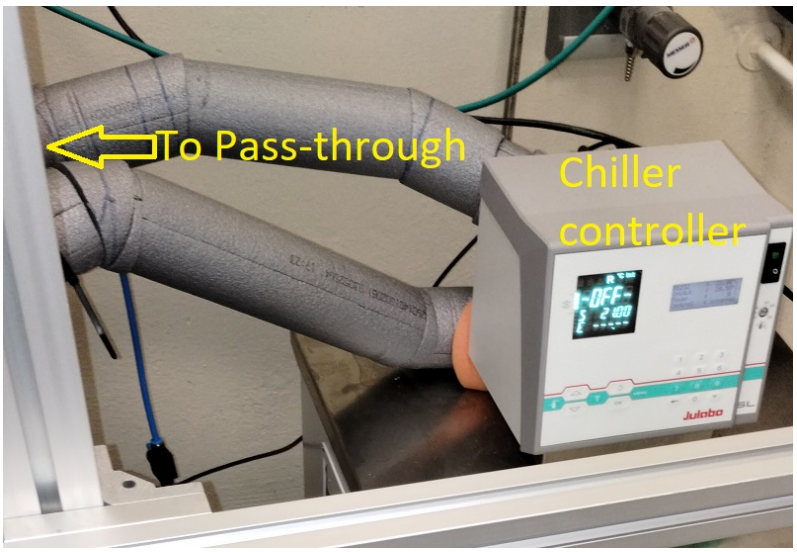

Figure 4.2: Chiller cooling routing.

4.3 Module periphery

From the module, two pigtails extend forward and backward out of the isolation box by passing between the window sill seal of the isolation bottom and the isolation hat (see figure 4.3).

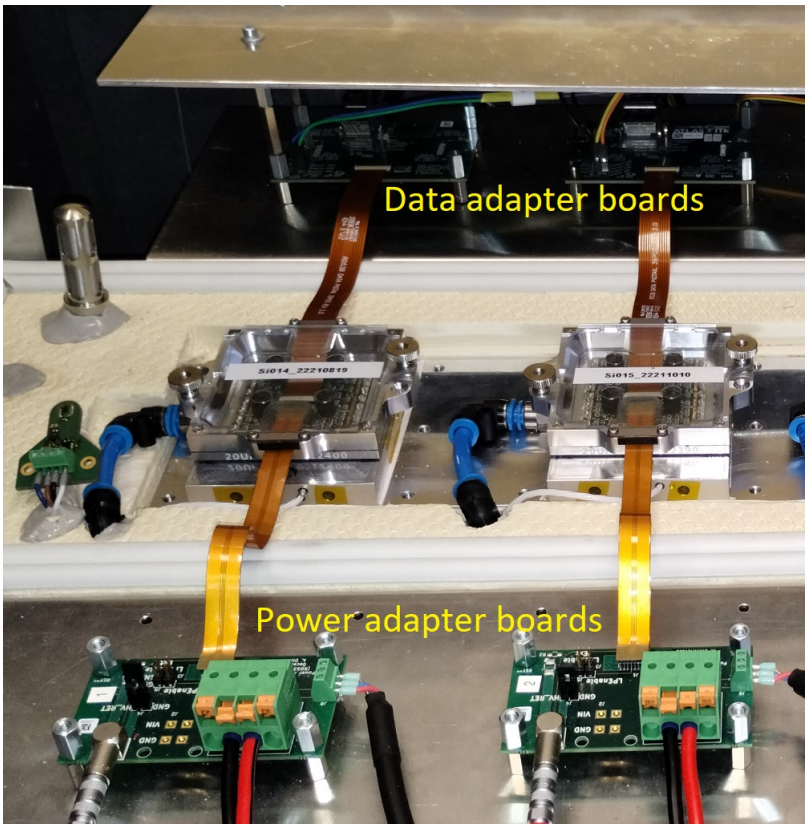

Figure 4.3: Module periphery for positions 1 and 2.

The pigtails connect to two adapter cards, one to supply power and return the NTC temperature, and the other to transport the communications lines and the analog chip feedback. The adapter cards are mounted on two bent aluminum sheets, level with the surface of the isolation bottom. On the power adapter (see figure 4.4 left) the jumper connecting the module ground with the HV ground is closed to allow for correct leakage current measurements. The 3-pin header of the NTC is replaced with a screw terminal to connect to the cRIO system. LV power is supplied with a custom power cable made by the electronics lab. The ground

cable is connected directly to the LV PSU and the live cable is connected to the HWI relay board and then to the PSU. On the data adapter (see figure 4.4 right) the pins for module ground and LV ground are connected via a jumper cable.

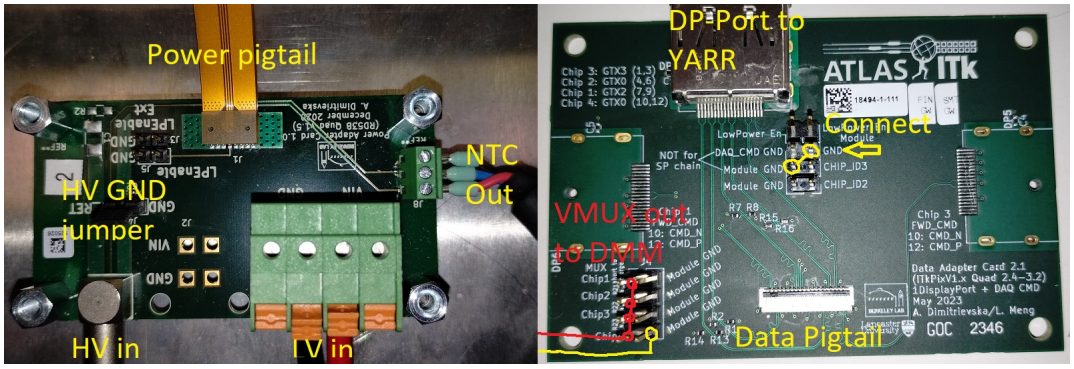

Figure 4.4: Pin-outs for the module adapter cards.

A pair of DMM readout cables are connected to the pins MUX_Chip_x and the neighboring module ground to allow for DMM readout of the module VMUX system. The display port of the adapter connects to the readout PC via a DP to mini-DP cable. During testing, one data transmission line in the data adapter in position 1 failed and during the installation of a module in position 2, the pigtail connector on the adapter broke mechanically. Both were replaced with new boards. An aluminum cover was added on top of the data adapter array to allow easy temporary storage of the isolation box hat during module installation into the test stand. This cover is held up by standoffs connected to the module adapter cards.

4.4 Vacuum system

Four vacuum chucks are mounted 115 mm apart on the cooling plate each using two M3 hex bolt screws. To aid the transfer of heat a ceramic heat transfer foil was placed between the VC and the cooling plate. The VCs are rotated in such a way the positioning grove of the carrier only allows the modules to be inserted in the correct orientation, data tail facing backward, and power tail forwards. The vacuum lines leave the VCs leftwards, get redirected with 90° connector forwards, and then leave the isolation box downwards with another 90° connector. Under-

neath the isolation bottom, each line connects to a switch, to allow the separation of the vacuum supply. After the switches, the lines are manifolded into one main line via 90° and T-adapter pieces. The main line has one split via a T-adapter to the cRIO vacuum sensor and the rest continues to the vacuum pump.

4.5 Dry-air system

The dry-air system went through three iterations during commissioning.

The first iteration used the pre-existing air dryer from the first pixel production. This system could not provide enough dry airflow to maintain the necessary dew-point of −35° C in the test stand. Additionally, it was discovered that the dryer was leaking oil. After an inquiry with the manufacturer, the dryer was found to be 2 years older than the maximum lifetime of this model. The system was dismantled and testing was continued with nitrogen instead of dry air until a new air dryer was procured and installed. With the new dryer installed in the basement, due to the noise of operation, and a new dry airline installed in the lab, the test stand was switched back to dry-air operations. The new dryer is an OFP SMART 0010 Superplus (see figure 4.5) installed in a air filter dryer combination by the company Donaldson that can supply up to $\approx 8\,\mathrm{m}^3/\mathrm{h}$ at 7 bar pressure.

It supplies oil- and dust-free dry air with a dew point of −75° C. Such a low dew point is necessary since the dry air will also be supplied to the climate chamber for thermal cycling, with cycles reaching −55° C.

4.6 Interlock system

The interlock system is based on the commercially available cRIO system. The electronics lab adapted the HWI on plans from the University of Glasgow. The HWI consists of the cRIO crate (figure 4.6) with its sensor card inserts, a custom power relay card, and a sensor accumulation PCB (figure 4.7).

The relay card allows the cRIO system to cut power to specific modules, regardless of the communication status with the PSUs. The sensor PCB accumulates the wires from the four NTCs, the environment sensor, lid switch, vacuum- and dry-air pressure sensors into a sub-d connection that is passed through the relay

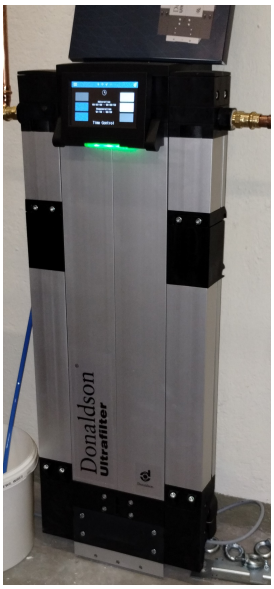

Figure 4.5: Donaldson Ultrafilter air dryer installed in the basement of University of Siegen Emmy-Noether-Campus Building A.

Figure 4.6: cRIO crate.

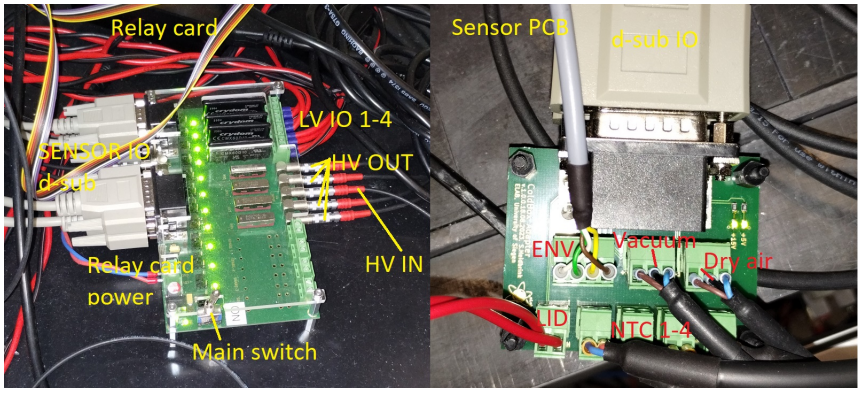

Figure 4.7: HWI relay card and sensor accumulation PCB.

card to the cRIO crate. The PT100 connections from the VC temperature sensors are connected directly to a cRIO interface card.

4.7 Source system

The source movement system was assembled as described in chapter 2. It was placed over the testing assembly, the motor functions were tested, and the module positions were pre-calibrated. The source within its casing, was placed into the source carrier and the first source scan was performed. This self-trigger source scan failed as the visible pattern was random and had far too few hits in comparison to the expected source strength. A noise scan/random-trigger-based source scan was performed to exclude a failure of the self-trigger system. This showed similar results. The new source system was removed and a variety of self-trigger source scans were performed with other Sr^{90} sources that were verified to work with previous module source scans. These scans worked within the limitation of these other sources, such as low activity or narrow beam cones. It turned out, that the source tablet was inserted into the custom aluminum casing facing away from the opening. The shielding blocked all but the negligible gamma line of the Sr^{90} source, causing the random low hit patterns of the self-trigger scans. Once the source was extracted, flipped, and reinserted into the casing, testing with the new source system could begin. The first self-trigger scans with the new source failed with noise warnings and a core corruption error within seconds of the scan

starting. A random-trigger-based scan runs properly and delivers workable x-ray like pictures of the flex within 30 s of scan time. This led to the knowledge that the self-trigger readout system fails under the design conditions due to trigger overflow. To combat this,a series of self-trigger source scans were performed while varying the source height and material the beam had to pass through to hit the module's sensor. Details of this investigation can be found in Mara Fries bachelor thesis [24]. The result was that the source needed to be placed at about 33 cm above the modules with a 200 μm thick sheet of aluminum inserted into the source carrier to attenuate the source's energy to allow for normal condition testing with the self-trigger system. Thus, the hit rate of the self-trigger scan is measured to be around 250000 hits per second and module. It leads to a scan time of 30 min to accumulate the required 10 hits per pixel in the power connector region of the module (see figure 4.8 for the current automated solution).

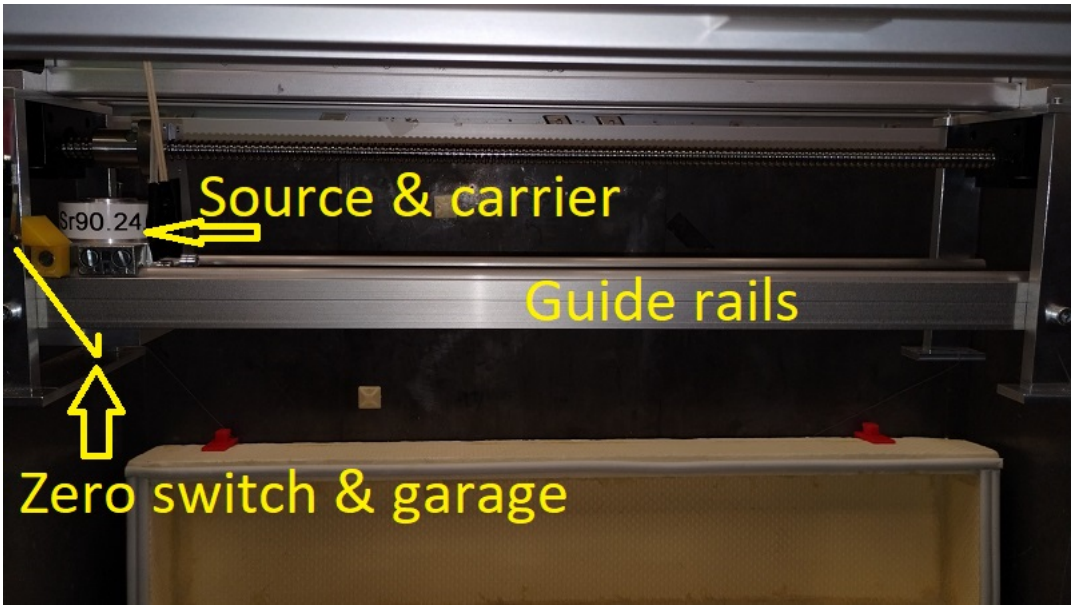

Figure 4.8: Source system of the test stand.

To be mentioned, the system was found to work without the described changes by running the source scan without HV, due to lowered sensor efficiency. A different approach to lower the activity of the source by placing material in between it and the module. This reduces the activity of the source by stopping the elec-

trons that do not possess the kinetic energy to pass through the material and then still trigger a hit. The problem with this is that the whole emission spectrum of the source is shifted to lower kinetic energies making it harder for the remaining electrons to penetrate thicker parts of the flex such as the connectors. With the necessary shielding (2.5 mm aluminum) to run scans the runtime exceeds 24 h to accumulate 10 hits per pixel under the connectors. This solution was this discarded since it requires too much time.

5 Conclusions and insights for future work

5.1 Summary

The goal of this thesis was to design and commission an ITk multi-pixel module test stand (figure 5.1) for the Siegen ATLAS pixel group.

I designed the necessary parts in CAD software, arranged the assembly of parts with our mechanical workshop, cleaned an existing testing setup enclosure for reuse, commissioned the test stand's hardware, set up the testing PC running Linux ALMA 9, see figure 5.2 left, and wrote custom Python code to allow for automated testing of up to four ITk quad pixel modules in series.

The custom testing script was designed to be used with minimal instructions as every step is done via user queries with all possible options visible in the terminal. Once automated testing is started, no further user input is necessary. The script will continue to the next module if an error occurs. Actions by the script and errors are logged for later review with a time stamp. Since commissioning, 18 RD54b quad modules passed through the QC process. With the help of other users, along with the data supplied by the test stand, we aim to fully qualify the test stand for the production of the ATLAS ITk pixel detector modules by the second half of this year. Currently, the test stand allows automated quality control for up to four quad modules of either the RD53b or the ITkPixV2 readout chip variant. This process takes around 2.5 hours per QC step with two initial QC steps necessary per module. The full QC of four modules currently lasts around 20 hours.

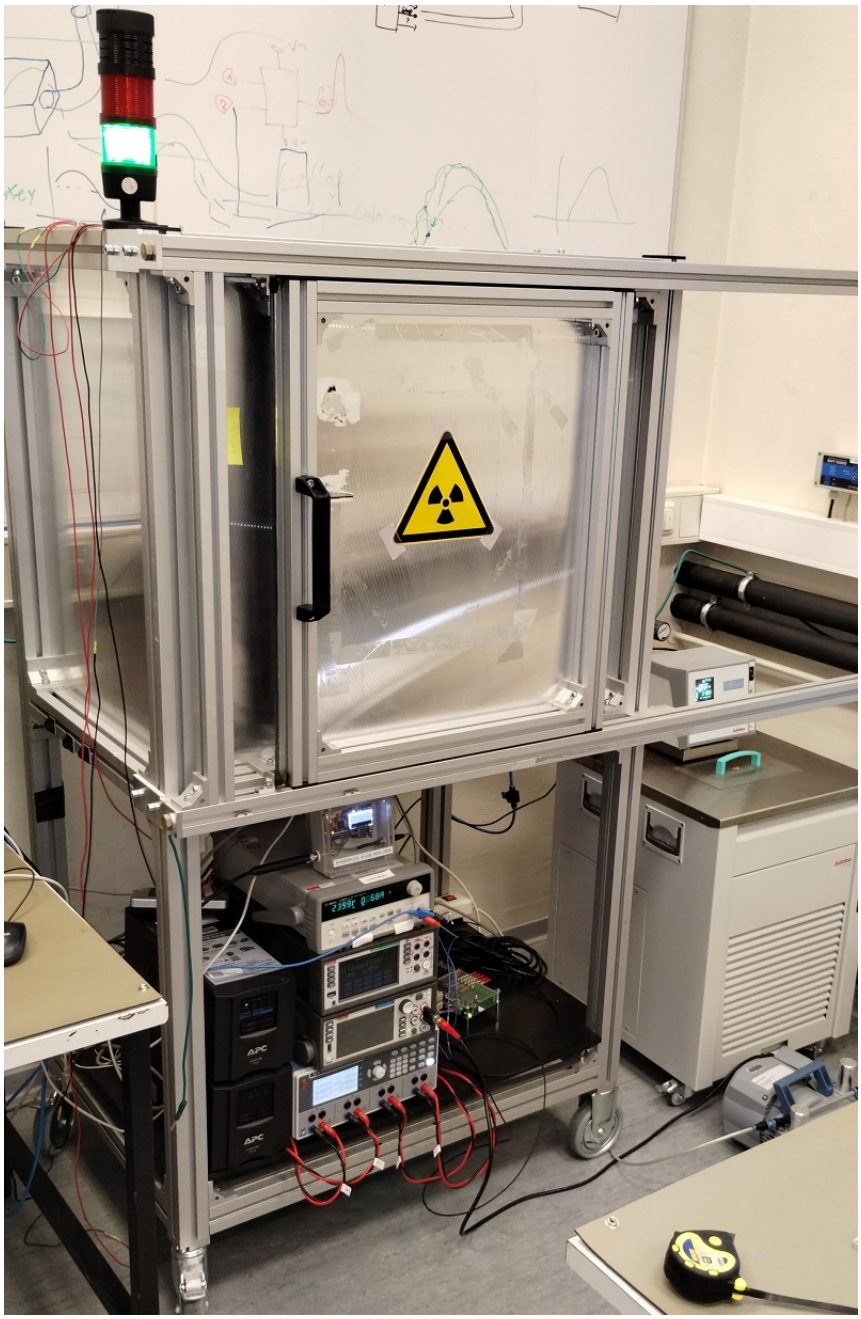

Figure 5.1: Visible is the shielded enclosure with the periphery stack and HWI hardware below, and the chiller and vacuum pump to the right of the stand.

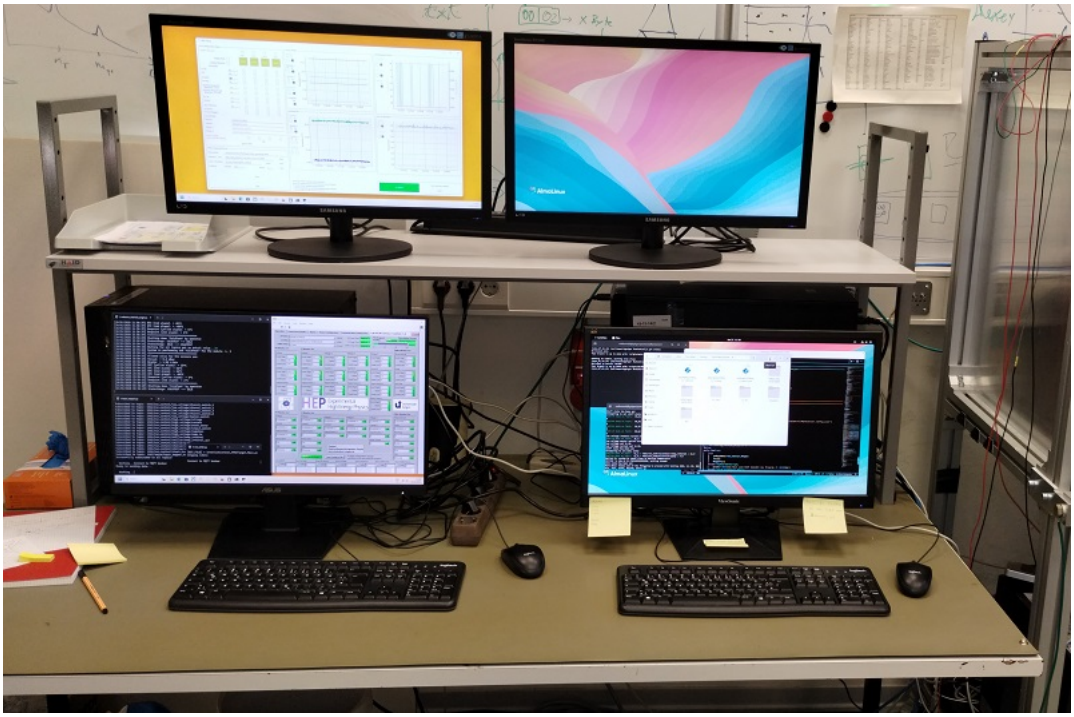

Figure 5.2: The HWI and testing PCs.

5.2 Future work

While the test stand is now complete and ready for testing, there is already future work visible, such as adapting the QC process to the specifications of the ITkPixV2, which has yet to be released by the collaboration. Adding more automated functions to the test stand allows for automated testing of later module qualification steps. The current scripts fulfil the requirements for the initial QC testing in both, warm and cold conditions. However, some testing needs to be repeated after the module coating and after the thermal cycling. The script has not yet ben adapted, as requirements are still under development for these steps in the module QC process.

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6 Appendix

6.1 Code repository

The code described in this thesis is available here:
https://github.com/NicoMalinowski/RunControl.git

6.2 Device list

D01 Chiller: Julabo FP51 SL

D02 Air dryer: OFP SMART 0010 Superplus

D03 LV PSU: Rohde & Schwarz HMP 4040

D04 HV PSU: Keithley 2470 SourceMeter

D05 DMM: Keithley DMM 6500

D06 Multiplexer card for DMM: Keithley 2000-SCAN

D07 YARR FPGA card: TEF 1001 R2 with Ohio designed adapter

D08 cRIO System

D09 Stepper Motor: Lin Engineering 4118 Series

D10 Motor Controller: Lin Engineering R256

D11 Temperature and Humidity Sensor: Custom readout of HC2A-IC Probe

Selbstständigkeitserklärung

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