

UNIVERSITÄT SIEGEN

BACHELORARBEIT

**Dealing with core column issues on ITkPix modules for the
HL-LHC upgrade of the ATLAS detector**

Luke Hammer

Arbeit zur Erlangung des akademischen Grades
Bachelor of Science

vorgelegt der

Experimentellen Teilchen- und Astroteilchenphysik
Department Physik

Gutachter

Prof. Dr. Markus Cristinziani

Version vom
24. August 2026

Dieser Forschungsbericht wurde als Bachelorarbeit von der Naturwissenschaftlich-Technischen Fakultät der Universität Siegen angenommen. Seit der Annahme sind höchstens geringfügige Änderungen vorgenommen worden. Der wissenschaftliche Inhalt der Arbeit ist unverändert.

Angenommen am: 15.06.2026

1. Gutachter: Prof. Dr. Markus Cristinziani

Acknowledgements

This thesis was a lot of work, work which I could not have done alone. I would like to thank all the people who helped me to finish this.

I would like to express my sincere gratitude to Prof. Dr. Markus Cristinziani for giving me the opportunity to work on this thesis and to contribute to such an exciting field of scientific research. I am particularly grateful for the opportunity to gain valuable experience beyond the scope of this thesis, including participation in scientific conferences and collaboration within an international research environment.

I would also like to thank Dr. Wolfgang Walkowiak for his continuous support throughout the preparation of this thesis. His encouragement, advice, and willingness to help whenever needed were greatly appreciated.

Furthermore, I am grateful to my friends, both within and outside the university, for their support during my studies. Their discussions, encouragement, and companionship helped me overcome challenges, while also providing a welcome balance to academic life.

Finally, I would like to thank my family for their unwavering support throughout my entire academic journey. Their trust, encouragement, and belief in me have made it possible for me to pursue my studies and complete this thesis.

To all of them, I offer my sincere thanks.

Contents

1	Introduction	1
2	The ATLAS ITk pixel detector	3
2.1	The current ATLAS detector	3
2.2	The ATLAS detector at the HL-LHC	5
2.3	Pixel modules for the ITk detector	6
2.3.1	General structure	6
2.3.2	Readout architecture	8
3	Core column issues	11
3.1	Definition and symptoms of core column issues	11
3.2	Tools for core column diagnosis and mitigation	13
3.2.1	Core column scan	13
3.2.2	Core column bash script	13
3.2.3	GUI tool for manual core column masking	14
3.3	Current situation in the ATLAS ITk	16
4	Core column investigation in Siegen	19
4.1	Electrical test setup in Siegen	19
4.2	Core column investigation on ITkPix v2 (RD53C) modules	20
4.3	Core column investigation on ITkPix v1.1 (RD53B) modules	25
4.4	Optimised workflow for problematic modules	30
4.5	Correlation of core column issues with wafer position and dicing quality	30
4.6	Sensor cleavage	33
4.7	Core column issue statistics in Siegen	34
5	Conclusion	35
	Bibliography	37
	List of Figures	39
	List of Tables	41

Introduction

The Standard Model (SM) of particle physics is the best available description of the fundamental particles and forces in the universe [1]. It incorporates the elementary particles that constitute matter as well as the gauge bosons that mediate the strong, weak, and electromagnetic interactions. To investigate these particles' properties, their interactions, and possible theoretical frameworks extending the SM, experiments require an environment of high-energy particle beams and precise measurement systems.

For exactly this purpose, the Large Hadron Collider (LHC) was constructed at CERN in a tunnel with a circumference of 26.7 km originally built for LEP (Large Electron–Positron Collider) [2]. The LHC currently operates at a centre-of-mass energy of 13.6 TeV for proton–proton collisions during its third operational phase, also known as Run 3 [3]. In this two-ring superconducting hadron collider, proton beams are accelerated to near the speed of light and brought into collision at four specific interaction points.

At one of these four interaction points at the LHC, ATLAS is one of the two general-purpose detectors designed to probe these high-energy collisions [3][4]. It is the largest particle detector by volume ever constructed at a particle accelerator, measuring about 44 m in length and 25 m in height, with a total weight of approximately 7000 t. The ATLAS detector uses a cylindrical, onion-shell-like layout of concentric layers consisting of the inner detector (ID), the calorimeters, and the muon spectrometer. The discovery of the Higgs boson in 2012 by the ATLAS and CMS experiments marked a major milestone in particle physics, confirming the Higgs mechanism and completing the particle content of the SM [5][6].

To further extend the discovery potential in the future and to study even rarer physics processes beyond the current LHC's capabilities, the collider will undergo a major upgrade in the years after finishing Run 3, starting July 2026, to become the new High-Luminosity LHC (HL–LHC) [7]. The overall LHC/HL–LHC schedule is shown in Figure 1.1. With this upgrade, the instantaneous luminosity will reach $5\text{--}7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$, delivering an integrated luminosity of $3000\text{--}4000 \text{ fb}^{-1}$ over a decade of operation. Challenges introduced by this upgrade are increased pile-up in the detector, with up to 200 proton–proton collisions per bunch crossing, and increased radiation levels in the innermost detector regions.

The current ID was not designed for high radiation levels and large data rates expected at the HL–LHC. It will be replaced with a new all-silicon Inner Tracker (ITk) to maintain tracking performance in the HL–LHC environment [8]. The ITk system will consist of two primary components, a high-granularity

pixel detector in the innermost region and a large-area strip detector surrounding it. The pixel detector will increase the number of layers and significantly extend tracking coverage up to a pseudorapidity of $|\eta| = 4.0$ in comparison with the current ID coverage of $|\eta| = 2.5$.

Constructing a tracker of this magnitude with over 10 000 hybrid pixel modules requires a geographically distributed production model involving multiple industrial partners and institutes [9]. As one of these specialised production and testing sites, the University of Siegen is actively involved in the assembly and quality control (QC) of pixel modules. This work ensures that the modules meet the ATLAS detector requirements for operation at the HL-LHC.

During the electrical testing of both, pre-production and production ATLAS ITk pixel modules, characteristic inefficiencies referred to as core column (CC) issues have been identified in those modules [10]. This failure mode, which can cause chips to continuously send faulty data or to stall the readout system, affects approximately 20 – 25 % of ITk pixel modules.

In this thesis, dedicated studies of pixel modules affected by core column issues are presented. The goal is to develop an optimised workflow to deal with affected modules and thus improve the module yield during production and electrical testing.



Figure 1.1: Overview of the LHC schedule, including the current upgrade plan to go from the LHC to the HL-LHC [11].

The ATLAS ITk pixel detector

2.1 The current ATLAS detector

The ATLAS detector at the LHC is located in its underground experimental cavern at Interaction Point 1 [3]. The apparatus is a large-volume particle detector, measuring approximately 44 m in length and 25 m in height with an overall weight of around 7000 t [4]. With respect to the interaction point, the detector is nominally forward–backward symmetric. A right-handed coordinate system can be defined with its origin at the IP at the centre of the detector [3]. The z -axis is aligned with the beam pipe, the x -axis points from the IP to the centre of the LHC, and the y -axis points upward. In the transverse plane, cylindrical coordinates (r, ϕ) are used, where ϕ describes the azimuthal angle around the z -axis. The polar angle θ is measured from the beam axis, which is typically expressed in terms of the pseudorapidity, defined as

$$\eta = -\ln \left[\tan \left(\frac{\theta}{2} \right) \right]. \quad (2.1)$$

The spatial arrangement of the detector components is closely linked to the magnetic field configuration required for particle tracking and momentum measurement.

The ATLAS detector comprises a hybrid system of four large superconducting magnets. These magnets extend up to 22 m in diameter and 26 m in length [4]. The central solenoid is aligned with the beam axis and surrounds the ID cavity. It provides a 2.0 T axial magnetic field for momentum measurement within the tracking volume. The toroid magnets are used to measure muon momenta within the large volume of the muon spectrometer. They consist of one barrel toroid and two end-cap toroids. The barrel toroid provides a field of approximately 0.5 T, while the end-cap toroids produce a field of approximately 1.0 T for the outer muon system. This composition of magnets serves as the framework for the subdetector layers, which are placed in distinct regions between and inside the magnetic system.

The cylindrical, onion-shell-like layout of the ATLAS detector is shown in Figure 2.1. The ATLAS detector consists of three concentric subdetectors: the ID, the calorimeter system, and the muon spectrometer [3]. As the primary tracking device, the ID is designed to reconstruct the trajectories of all charged particles, measure momenta, and identify vertices. The ID is integrated within a cylindrical envelope measuring 7.02 m in length and 1.15 m in radius. It covers the pseudorapidity range $|\eta| < 2.5$. The innermost system, the pixel detector, performs high-granularity measurements

for vertex reconstruction. It consists of three barrel layers of pixel modules, each with a pixel size of $50\,\mu\text{m} \times 400\,\mu\text{m}$. An additional layer, the Insertable *B*-Layer (IBL), was installed close to the beam axis between LHC runs 1 and 2. Silicon sensors in the IBL are located at a nominal radius of 33.5 mm. The pixel size in the IBL is $50\,\mu\text{m} \times 250\,\mu\text{m}$. All four layers together result in a total of 92 million pixel readout channels in the ID. The second component of the ID is the semiconductor tracker surrounding the pixel detector, utilizing silicon microstrip technology to provide typically eight measurements per track. As the outermost component of the ID, the transition radiation tracker uses gas-filled straw tubes for continuous tracking and enhanced electron identification. Located outside the solenoid, the calorimeters are designed to absorb charged and neutral particles. Particles initiate electromagnetic or hadronic showers in the calorimeters, depositing part of their energy in the active material. Only this fraction of the total energy is directly measured. The particles' energies and positions are then reconstructed from the calibrated detector response. The calorimeter system uses two different technologies. It utilises liquid Argon (LAr) technology for electromagnetic measurements covering $|\eta| < 3.2$. For hadronic calorimetry in the barrel, scintillating tile technology is used, with coverage $|\eta| < 1.7$. In the hadronic end-cap calorimeters, LAr technology is also used. The muon spectrometer (MS) is the outermost detector system and is designed to detect muons exiting the calorimeters. Their momenta are measured via their deflection in the toroidal magnetic field. The MS covers the range $|\eta| < 2.7$.

Under the challenging conditions of run 3, the technical design and arrangement of these subdetectors allow the ATLAS experiment to maintain excellent physics performance. The LHC currently operates at a centre-of-mass energy of 13.6 TeV [3]. An instantaneous luminosity of $2 \times 10^{34}\,\text{cm}^{-2}\text{s}^{-1}$ is sustained with an average of up to 60 proton–proton collisions per bunch crossing. After including the IBL inside the ID for run 2, a significant improvement in vertex reconstruction was achieved. While the ATLAS detector continues to perform well, the current peak luminosity of the LHC is approaching its operational limits. These are primarily set by luminosity-induced heating of the inner triplet magnets. They focus the beams before they reach the interaction point. The current ID is affected by cumulative radiation damage to its silicon sensors over its years of operation. It was not designed to withstand the upcoming radiation levels and data rates of the future HL–LHC. Given these limitations, the current ID will be replaced by an all-silicon ITk for the HL–LHC era.

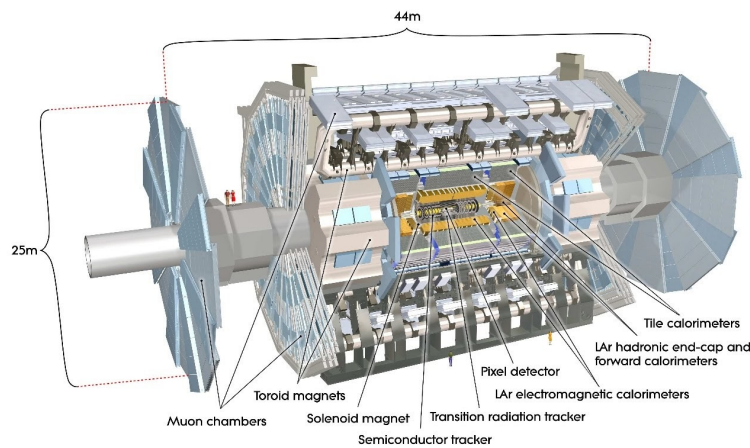


Figure 2.1: Cut-away view of the current ATLAS detector, showing its different components and their scale [4].

2.2 The ATLAS detector at the HL–LHC

The HL–LHC is planned to start operation in June 2030 [12]. The project aims for an instantaneous luminosity of $7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ [8]. This corresponds to an integrated luminosity of $3000 - 4000 \text{ fb}^{-1}$ over a runtime of approximately 10 years. A further operational challenge is the resulting large pile-up in the detector. About 200 proton–proton interactions are expected per bunch crossing.

The ITk system will consist of a high-granularity pixel detector surrounded by a large-area strip detector. Figure 2.2 shows a schematic 3D layout of the ITk. The extended tracking coverage up to a pseudorapidity of $|\eta| = 4.0$ improves detector performance, particularly in the forward region. The geometric coverage is illustrated in the technical r – z layouts in Figure 2.3(a). The pixel detector consists of a barrel and end-caps. The barrel comprises five cylindrical layers, complemented by end-cap rings. Due to the expected large cumulative radiation damage at small radii, the innermost two layers are designed to be replaceable during the detector lifetime [13].

The successful operation of the ITk pixel detector depends on approximately 10 000 individual hybrid pixel modules [9]. These modules constitute the fundamental mechanical and electrical building blocks of the detector. The production of these hybrid pixel modules is distributed among multiple industrial partners and research institutes, depending on the production step. At the University of Siegen, at least 200 quad pixel modules for the Outer Barrel (OB) of the pixel detector will be produced. The OB comprises the outer three layers of the five-layer pixel barrel illustrated in Figure 2.3. A specialised module design and a high-bandwidth readout architecture are essential to handle the large data rates expected in these layers [13]. The following section details the general structure of these pixel modules and the specialised logic governing their readout.

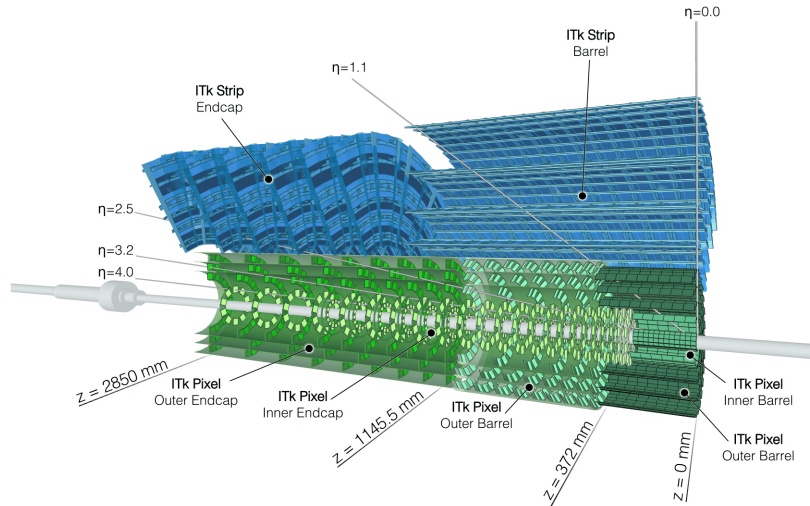


Figure 2.2: A schematic 3D longitudinal view of the ITk system, illustrating the nested barrel and end-cap structures for both the pixel (green) and strip (blue) subdetectors [14].

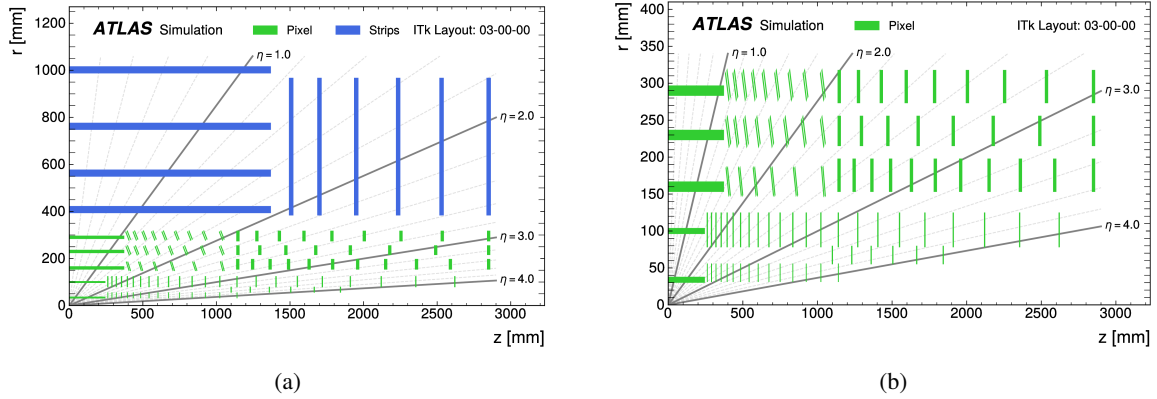


Figure 2.3: Technical r - z layouts of the ITk detector, illustrating the extended tracking coverage up to $|\eta| = 4.0$. (a) Schematic view of one quadrant, showing the active elements of the pixel and strip subdetectors. (b) Detailed view of the pixel detector quadrant, highlighting the five-layer barrel layout [14].

2.3 Pixel modules for the ITk detector

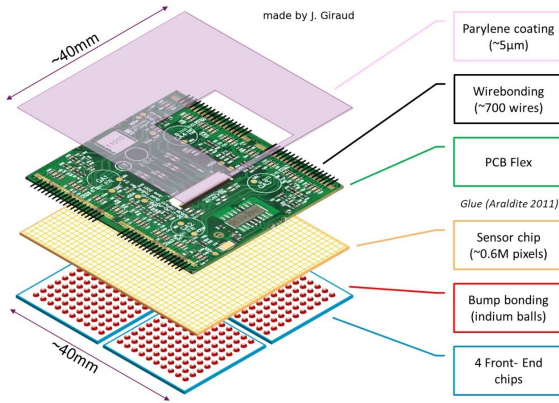
2.3.1 General structure

The hybrid pixel module serves as the fundamental mechanical and electrical tracking unit in the ITk pixel detector. It consists of a high-resistivity silicon sensor and several front-end (FE) chips [9]. Production focuses on two primary types: triplet modules (3×1 chips) for the innermost layer and quad modules (2×2 chips) for the remaining layers [15]. Quad modules, which utilise a single planar $4 \times 4 \text{ cm}^2$ sensor tile, constitute approximately 95% of the modules. The University of Siegen is responsible for the assembly and testing of at least 200 quad pixel modules for the OB. To connect the sensor to the FE chips, the flip-chip bump-bonding technique is used. It connects the two components using AgSn solder bumps, which establish an electrical connection for each individual pixel cell. The combination of the sensor and FE chips is referred to as a bare module (BM). As a production site for the assembly and QC of pixel modules, the University of Siegen receives the BM and a flexible printed circuit board (PCB) as separate components. The flexible PCB is glued to the sensor's backside and wire-bonded to the FE chips. It provides the interface for power, including both low-voltage and high-voltage supplies, as well as clock and data signals. Passive components, such as decoupling capacitors and a negative temperature coefficient (NTC) thermistor, are populated on the flexible PCB. After module assembly and initial electrical testing, the modules are coated with a thin layer of parylene to ensure electrical isolation and environmental protection. A schematic of this vertically stacked layout and a photograph of a pixel module assembled in Siegen are shown in Figure 2.4. While this physical assembly establishes the mechanical and electrical integrity of the module, the functional performance is driven by the response of the silicon sensor to traversing charged particles.

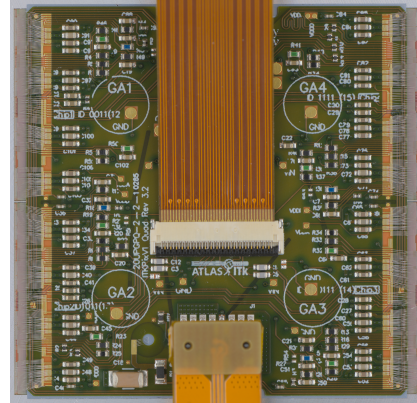
The detection process begins when charged particles traverse the high-resistivity silicon bulk and lose energy through inelastic collisions with electrons. The specific energy loss ($-dE/dx$) through ionisation of these particles is described by the Bethe-Bloch formula as a function of the particle's velocity and charge and of the material properties of silicon [16]. This energy transfer results in the creation of electron-hole pairs along the particle's trajectory through the silicon sensor. In silicon, the average energy required to produce a single electron-hole pair is approximately 3.62 eV. A

reverse-bias voltage of 120 V is applied across the p-n junction to create a sensitive depletion region [9]. In the resulting electric field, the electrons drift towards the segmented readout electrodes while holes move toward the global backside contact. The collected charge is transferred via the bump bonds to the analog front-end (AFE), where it is integrated and compared against a programmable threshold [13]. The outer barrel quad modules built in Siegen are tuned to approximately 1500 e. Signals exceeding this threshold are digitised using a 4-bit Time-over-Threshold (ToT) measurement, which provides a charge value proportional to the pulse width in units of 25 ns bunch crossing intervals. The production of such precise digital data at the large collision rates of the HL–LHC requires a highly granular detector design. This requirement is fulfilled by the specialised ITkPix readout chip, which is the ATLAS variant of the RD53 ASIC (Application-Specific Integrated Circuit). The ITkPix v1.1 and ITkPix v2 modules are based on the RD53B and RD53C ASIC versions, respectively.

The granularity of the tracker is significantly improved compared to previous generations to handle the large pile-up of the HL–LHC [9]. The ITkPix readout chip is fabricated in 65 nm CMOS (Complementary Metal-Oxide-Semiconductor) technology [13]. Each ITkPix chip contains 153 600 pixels organised into 400 columns and 384 rows. The chip dimensions are approximately $20 \times 21 \text{ mm}^2$. Standard pixel dimensions are $50 \times 50 \mu\text{m}^2$, while specialised $25 \times 100 \mu\text{m}^2$ pixels are utilised in the innermost barrel layer. In the current ID outer pixel layers, pixel dimensions of $50 \times 400 \mu\text{m}^2$ are implemented. The IBL uses $50 \times 250 \mu\text{m}^2$ pixel sizes, so the ITk upgrade of the ATLAS detector will result in much finer pixel granularity. To manage this immense pixel density, the ITkPix chip employs a highly structured internal organisation. The pixel matrix is subdivided into smaller logical units. This hierarchical internal organisation provides the structural framework for the readout at the large data rates of the HL–LHC environment. The design and functionality of this readout structure are described in the following subsection.



(a) Schematic of a quad pixel module (by J. Giraud).



(b) Photograph of an assembled quad pixel module.

Figure 2.4: Structural overview of an ITk quad pixel module. The schematic in (a) defines the layering of the internal components [15], while (b) shows the physical realisation of a module produced for the Outer Barrel.

2.3.2 Readout architecture

To manage the large hit rates of up to 3 GHz/cm^2 and a trigger rate of 1 MHz, the ITkPix chip utilises a hierarchical readout structure. The following description is taken from [13]. This design moves away from traditional global memory structures to a distributed approach in which hit processing and buffering occur locally within the pixel matrix. The internal hierarchy of this data flow is visualised in Figure 2.5.

The fundamental unit of digital processing is the pixel region, which consists of four pixels organised in a 4×1 array. Within these regions, asynchronous hits from the FE are synchronised to the 40 MHz bunch-crossing clock and digitised into a 4-bit ToT value. These data are stored in local latency buffers for up to $12.5 \mu\text{s}$ until a trigger signal is received.

The matrix is further organised into pixel cores, each containing 2×8 pixel regions corresponding to 8×8 pixels. These cores serve as the primary building blocks for the synthesised digital logic and include built-in buffers and skew compensation for time-critical signals such as the clock and charge injection.

The architectural backbone of the ITkPix readout is the division of the pixel matrix into 50 independent core columns. In the ATLAS implementation, each core column is composed of 48 vertically stacked pixel cores. Because every core contains 64 pixels (8×8), a single core column represents a unit of 3 072 pixels, or 2% of the entire chip area. All 48 cores within a column share a common pixel core readout bus. This shared bus connects the local latency buffers of the pixel regions to a dedicated column readout controller located in the Digital Chip Bottom (DCB). To maintain signal integrity over this distance, the digital logic inside the pixel cores ensures that the 40 MHz clock remains synchronised within 1 ns across the entire column. Data extraction is handled by a circulating readout token mechanism. When a trigger signal is received, the column controller initiates the readout and asserts the readout token into the core column. Pixel regions that have stored hit data matching the trigger timestamp wait for the arrival of this token before asserting their zero-suppressed data onto the readout bus. In this mechanism, the token passes through all pixel regions in one core column before returning to the DCB. A critical feature of this architecture is that every core column functions as an autonomous readout pipeline. Independent controllers allow the chip to concurrently extract data for different triggered events across different core columns. This significantly improves the effective readout rate.

Once triggered data reach the DCB, they are processed by End-Of-Column (EOC) logic and packaged into 64-bit frames. The final data stream is transmitted via four serial electrical links, each operating at 1.28 Gb/s. This configuration provides a maximum bandwidth of 5.12 Gb/s per chip, which is needed to handle the large data rates in the innermost tracking layers.

The structural integrity of the independent core columns and their associated readout buses is a critical requirement for stable chip operation and the overall detector performance. Because the readout bus covers such a large number of pixel regions, it is highly sensitive to radiation-induced degradation or mechanical damage [10]. If a token gets "stuck" or the logic fails within a single core column, the entire chip readout may stall, or the DCB may receive a continuous stream of faulty data. This specific failure mode is referred to as a core column issue. The following chapter defines these pathologies and presents the diagnostic tools used to identify them during module production.

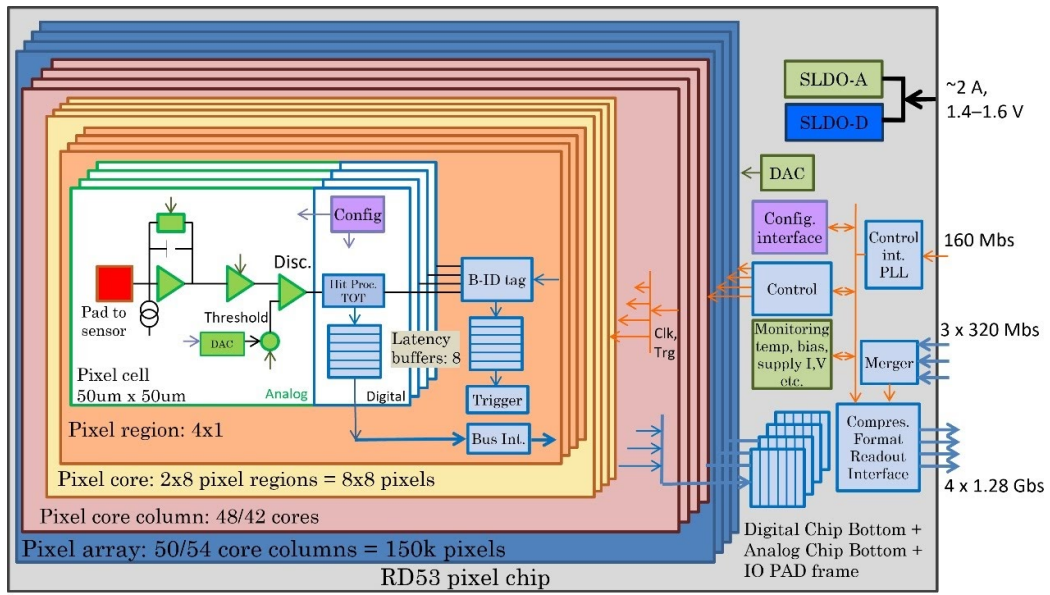


Figure 2.5: Schematic of the logical data flow architecture of the RD53 chip [13]. The values for the ATLAS implementation are shown on the left in the boxes (e.g., 48 cores, 50 core columns).

Core column issues

3.1 Definition and symptoms of core column issues

This section links the detector architecture described in Chapter 2 to the specific practical failures observed during module production. Individual chip malfunctions must be related to the QC criteria for assembled pixel modules. This is necessary to maintain a good module yield during production in Siegen. By detailing the erratic nature of the symptoms, this subsection motivates the description of specialised software tools and scripts. These tools are required for precise identification and mitigation of core column issues.

A core column issue refers to a characteristic chip malfunction in RD53 FE chips, in which the readout of the pixel module only works normally after specific core columns are disabled in the chip configuration [10]. As described in Chapter 2, masking a single core column results in the loss of 3 072 pixels, which correspond to 2% of the chip's active area. Currently, the QC criteria allow two disabled core columns per chip. Because of that, it is critical to minimise core column issues per chip by understanding the causes and mechanisms underlying these issues. There are different types of symptoms that indicate core column issues.

One observation during the electrical testing of pixel modules is that data loops time out during scans [10]. The extreme case of this observation is the chip's trigger processing logic entering a deadlock, in which scans are not able to finish and time out. This symptom occurs in various scan types and is difficult to distinguish from general communication failures unrelated to core column issues. If the readout is timing out or scans are not finishing, the operator has to identify whether this is caused by problematic core columns. A stuck readout could indicate a failure in the token-passing mechanism or the shared readout bus [13]. The second observation is the continuous transmission of so-called rubbish data [10]. During electrical testing, the DCB gets continuously flooded with this rubbish data. This results in unpredictable hit patterns on the affected chip occupancy maps during electrical testing. An example is given in Figure 3.1, where two digital-scan occupancy maps are shown for one chip 0x207c9 of module Si021. In a digital scan, 100 test pulses are injected into the digital logic of the FE chips for each individual pixel. It is an efficient check of whether the token-passing mechanism and the digital logic are working as intended. The expected value for a perfectly working chip is exactly 100 hits per pixel. In Figure 3.1(a), most pixels are read out with 100 hits. However, there is also a pattern on this occupancy map, as well as two small pixel clusters on the left and right chip edges. Those two pixel clusters consist of potentially broken or noisy pixels. This

already hints at a possible defect in the corresponding readout buses in these specific core columns. In Figure 3.1(b), similar scan results are displayed, but now the outer two core columns have been disabled in the chip configuration file. After masking those core columns, the rest of the chip no longer shows an unexpected pattern, and all pixels receive the intended 100 hits. Such behaviour can happen, for example, if the core column bus is damaged, which can have multiple causes, such as mechanical damage or a defect in the electronics of the readout chip.

These symptoms show erratic behaviour depending on various settings [10]. Chips might behave differently during electrical testing in "warm" ($\approx +20^\circ\text{C}$ NTC temperature) or "cold" ($\approx -15^\circ\text{C}$ NTC temperature) environments. Some core column issues might only appear during warm electrical characterisation or vice versa. Core column issues often depend on specific scan settings, such as the threshold value or the amount of injected charge. For example, a chip may show a poor occupancy map at a small injection charge of 1 650 e but appear fully functional at a large injection charge of 2 600 e [10]. Such dependencies indicate that the issue is not a simple permanent break but may involve marginal signal integrity or noise sensitivity.

Recent large-scale investigations within the ATLAS ITk collaboration confirm that the core column issue affects approximately 25% of production modules, representing a significant yield bottleneck [17]. Evidence from destructive testing indicates that these defects originate from mechanical damage sustained during hybridisation, specifically from silicon shards or edge chipping introduced during the dicing process. Furthermore, studies by Hultquist et al. demonstrate that more granular masking—such as disabling individual pixel cores—is often unstable, necessitating the disabling of entire core columns to ensure reliable front-end communication.

This erratic nature and the inconsistency of failure modes across various scan types are major challenges in the development of automated software tools to deal with core column issues. However, for around 10 000 pixel modules, which will be needed for the future ITk, automated identification of problematic core columns is necessary. Dedicated tools are required to identify core column issues on problematic chips and to verify whether a chip's communication is restored after specific core columns are masked. The following sections describe the three tools currently used in production at Siegen.

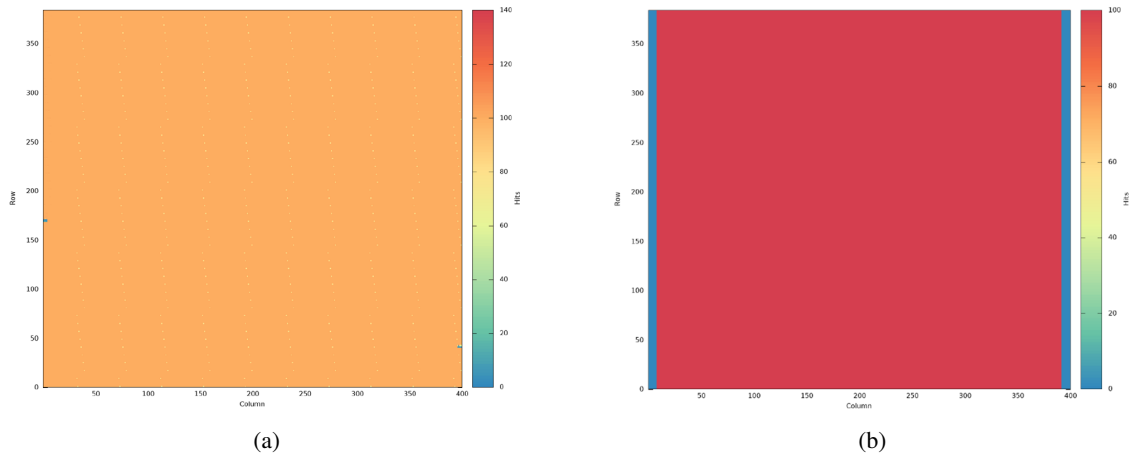


Figure 3.1: Digital-scan occupancy maps for chip 0x207c9 of module Si021. The occupancy map in (a) is an example of a core column issue symptom: the transmission of so-called rubbish data. Panel (b) illustrates how masking problematic core columns can eliminate readout congestion and recover overall chip operation.

3.2 Tools for core column diagnosis and mitigation

3.2.1 Core column scan

The first tool to deal with core column issues automatically is the core column scan [18]. Its purpose is to identify and automatically disable malfunctioning core columns during electrical QC to restore stable chip operation. The core column scan developed by the ATLAS Collaboration is integrated as a standard diagnostic scan within the YARR (Yet Another Rapid Readout) software. This YARR software is also distributed by the ATLAS Collaboration and provides a framework for electrical testing of pixel modules. During the core column scan, the chip responsiveness is tested core column by core column rather than testing the full matrix at once.

The scan is structured as follows. Unlike a digital scan, the charge injection is analog, resulting from `name = AnalogScan` and `InjDigEn = 0`. The key component of the core column scan is the loop `Itkpixv2CoreColLoop`, which runs over all 50 core columns on a chip (`min = 0`, `max = 50`, `step = 1`, `nSteps = 50`). Only the currently tested core column is enabled (`disableUnused = true`), and previously disabled core columns are also excluded (`ignoreDisabled = true`). A second loop, the parallel mask loop `Itkpixv2ParMaskLoop`, is used to distribute the injection over subsets of pixels via 16 mask steps (`min = 0`, `max = 16`, `step = 1`). For triggering, a third loop `Itkpixv2TriggerLoop` is implemented, which uses internal triggering (`extTrigger = false`). After collecting the data, the analysis algorithm here is `OccupancyAnalysis` with the argument `coreColMask = true`. This enables the automatic core column masking logic. The analysis evaluates occupancy data and identifies core columns failing a specified occupancy criterion. If more than 10% of pixels do not return the expected 100 hits, the core column is masked by the core column scan. At the end of the core column scan, several maps are created. The most important output for diagnosing core column issues is the occupancy map, which is used to check whether masking specific core columns leads to a clean chip response.

With the core column scan included in every full electrical test routine, this is a first step towards improving the production yield of modules with malfunctioning core columns. However, the core column scan is also limited in its application. If the overall chip communication is too unstable, which could even be induced by problematic core columns, the scan may not complete. No timeouts are implemented inside the scan configuration. This can block the production flow for modules with problematic core columns. As described above, core column issues depend on the threshold, the injection charge, and the temperature during electrical testing. A core column could be stable during the core column scan, but unstable during a different scan. Small numbers of noisy or hot pixels below the critical threshold can already lead to the known failure modes; however, those core columns are not masked by the core column scan. Therefore, the scan is useful as a first automated diagnostic step, but further tools are necessary to deal with more severely affected modules.

3.2.2 Core column bash script

The second tool provided by the ATLAS Collaboration to deal with core column issues is the core column script [18]. This bash script was developed to address the limitations of a single core column scan. The core column script is more of an enhanced verification wrapper than a complex algorithm itself. It automates and stabilises the application of the existing core column scan.

Before running core column scans, the core column script executes a preliminary check, namely

the `Itkpixv2ColumnTest` included in the YARR software. This specialised test was designed to verify the token-passing protocol and the vertical readout bus in each core column. During the test, no charge is injected and a timeout of 100 s is applied. After this first robustness check of the readout architecture, a core column scan is executed. The implementation of a 300 s timeout during the core column scan is another advantage over the single scan. The procedure of running the preliminary check and a core column scan is repeated five times.

The core column script is useful for problematic modules that cannot finish the core column scan. The preliminary `Itkpixv2ColumnTest` helps disable problematic core columns before executing the core column scan. Repeating the preliminary test and the scan five times improves masking reproducibility compared to a single core column scan. As a fail-safe automation, the implemented timeouts prevent stalled hardware from blocking the production flows. The core column script still has some limitations. In cases where modules show severe communication failure, even the automation script may time out because the problematic core columns are not detected by the preliminary check. Another limitation is the threshold set for each core column. If fewer than 10% of pixels in a core column cause readout issues, the core column is usually not identified and masked by either tool in the YARR framework. Especially in cases in which the number of problematic pixels causing a core column issue is less than the threshold value, another tool was developed. A GUI (Graphical User Interface) tool helps to manually mask exactly suspicious areas on the chip via the chip's configuration by an operator.

3.2.3 GUI tool for manual core column masking

The third tool for addressing core column issues is a GUI developed by Berkeley and Göttingen [19]. It is necessary to deal with problematic modules that cannot be handled by either of the two automated tools, the core column scan or the core column script.

The GUI-based masking tool provides an interface for operators to modify chip configuration files controlling the readout logic of the pixel matrix. It displays a grid corresponding to the 50 independent core columns of the FE chip. The core column masking configuration of the FE chip is given inside its `.json` configuration file and encoded in four registers (`EnCoreCol0`, `EnCoreCol1`, `EnCoreCol2`, and `EnCoreCol3`). This `.json` file is used as an input to the GUI masking tool. The current core column configuration is indicated by black cells in the grid. Together with the configuration file of the chip, the occupancy map of a previous scan result can be displayed as a background layer in the GUI tool. The operator is then able to inspect the occupancy map in the background, identify suspicious clusters of pixels, and select a new core column masking configuration. After selecting a new masking configuration and saving it, the GUI tool automatically updates the core column register values in the corresponding chip configuration file. In Figure 3.2, an example of the use of the GUI tool is displayed. A chip configuration was loaded together with its digital-scan occupancy map. The leftmost core column was disabled before using the tool, likely by one of the automated tools described above. An operator might now identify a hot pixel region in core column 34. If this module shows symptoms of core column issues, the operator could mask core column 34 and electrically test the module again.

An advantage over automated tools is that the operator can now locate and mask suspicious groups of pixels inside core columns where the number of pixels is below the threshold. This tool can be used for modules that behave differently in warm and cold testing environments. A module might pass QC criteria in warm testing and fail the same routine at lower temperatures or vice versa. In those cases, the operator is able to inspect the core column masking configurations together with scan occupancy

maps to find a new masking configuration. This GUI tool may provide the only practical way to recover problematic modules that cannot finish core column scans in time. Even if no suspicious pixels are observed but the module shows core column symptoms, it can be debugged by an operator. Debugging of such modules is time-consuming because it involves trial and error until a masking configuration is found to ensure stable module operation. In those cases, the GUI tool simplifies this iterative process for the operator. However, manual masking is significantly more time-consuming than automated tools and must be performed by an experienced operator. It is not feasible to determine core column masking configurations manually for around 10 000 pixel modules in the ITk project [9]. The GUI masking tool is used only for modules that show core column issue symptoms and cannot be handled by either the core column scan or the core column script in an automated way.

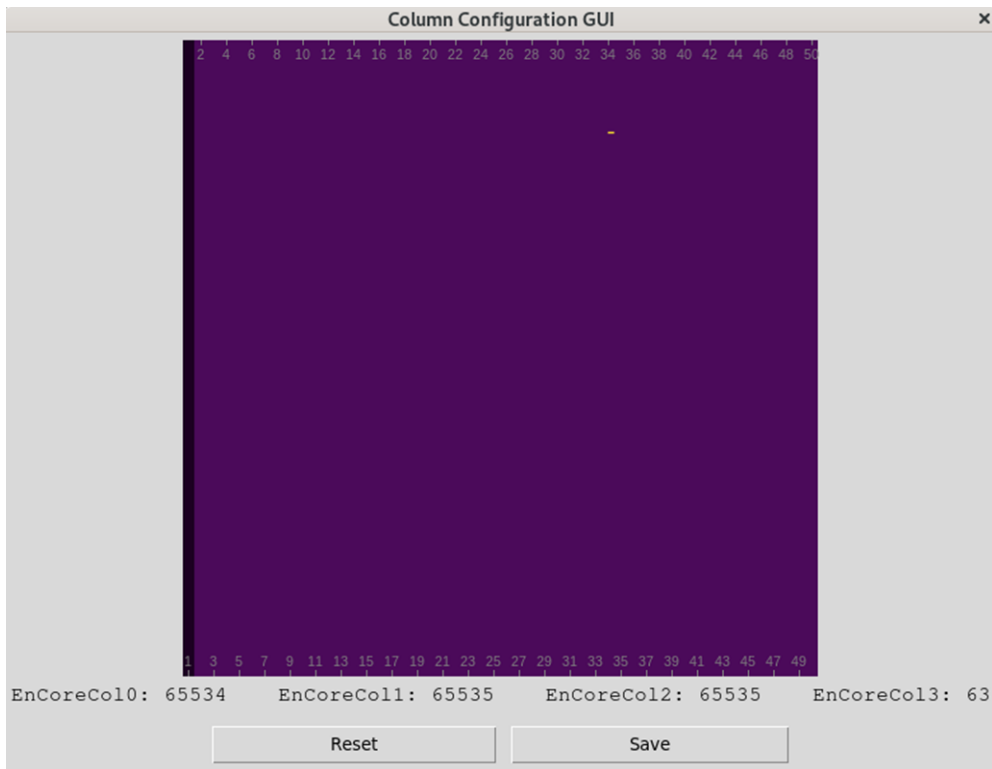


Figure 3.2: The GUI tool for manual core column masking for a single chip. The operator can view the current core column configuration or select a new set of core columns to mask manually. An occupancy map of a previous scan is displayed as a background layer to identify clusters of suspicious pixels.

3.3 Current situation in the ATLAS ITk

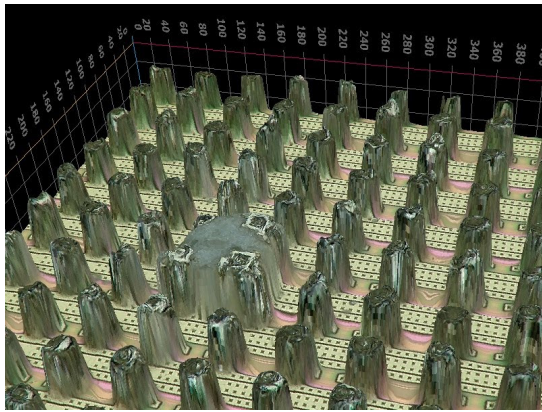
This section transitions from the functional description of tools for addressing core column issues to the global scale of the defect within the ATLAS ITk project. The issue has been observed across both pre-production ITkPix v1.1 (RD53B) and production ITkPix v2 (RD53C) chips [10]. Data extracted from the ITk production database and reported by L. Meng et al. are listed in Table 3.1. In this statistic, both quad and triplet modules are included. In the warm testing environment, chips and modules appear more likely to be affected by core column issues. As there are fewer modules in cold stages than warm stages, some modules with core column issues might not yet have progressed through the production chain. Warm testing stages precede cold testing stages, so problematic modules with many core column issues might not be tested in a cold environment yet. As stated above, modules behave differently under different temperatures. Sometimes, more core column issues occur in a warm environment; sometimes in a cold environment; there is no clear systematic pattern. In addition, the fractions of affected chips and modules are not negligible. The core column issue will have an impact on overall module production yield, and therefore its origin needs better understanding.

Design flaws as an origin of core column issues are considered unlikely. There are no intrinsic issues with the RD53 FE chip design because the affected chips were classified as fully functional during wafer probing [10]. Evidence suggests the core column issue originates during the post-wafer processing stages, specifically dicing and flip-chip bump-bonding. Affected modules have been disassembled, and silicon shards or other debris have been found at locations corresponding to disabled core columns. An example of a silicon shard located between multiple bump bonds after disassembly of a bare module is displayed in Figure 3.3(a). This silicon shard corresponds to a disabled core column in electrical testing and is most likely causing this core column issue. The distribution of the core column positions in Figure 3.3(b) shows that disabled core columns are more likely to occur at chip edges than elsewhere in the chip. This might be related to mechanical damage induced during dicing at the hybridisation vendors. In addition, microscopic cracks in the silicon of the FE chip have been observed that are related to core column issues. Currently, mechanical damage is considered the most likely cause of core column issues. This damage can be introduced at the hybridisation vendor during flip-chip bump-bonding or dicing. However, this can also happen because of damage during handling at other institutes, since the bare module, especially the thin silicon sensor, is fragile.

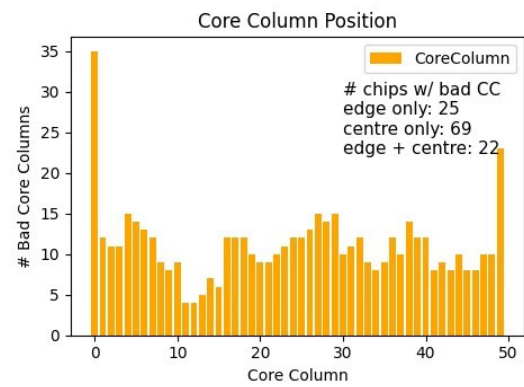
Those global statistics and pathologies reported by the ATLAS Collaboration provide the framework for evaluating specific modules regarding core column issues in Siegen. The following chapter details how the dedicated tools described above are used to address issues in affected modules at Siegen. The goal is to develop an improved workflow for electrical testing of modules with core column issues.

Table 3.1: Published statistics of modules and chips affected by core column issues, extracted from the ITk production database by L. Meng et al.. The warm testing regime is around $+20^{\circ}\text{C}$ and cold testing around -15°C module NTC temperature. Adapted from Ref. [10].

Chip version	Temperature	Affected modules	Fraction (%)	Affected chips	Fraction (%)
v1.1	Warm	77 / 357	21.6	116 / 1393	8.3
v1.1	Cold	42 / 249	16.9	57 / 982	5.8
v2	Warm	17 / 118	14.4	25 / 470	5.3
v2	Cold	9 / 85	10.6	12 / 340	3.5



(a)



(b)

Figure 3.3: In panel (a), a pixel module was disassembled, and debris was found between multiple bump bonds. This debris was found at a position corresponding to a disabled core column in the pixel matrix. The histogram in (b) displays the distribution of the positions of the core columns that were masked during electrical testing. Figure adapted from [10].

Core column investigation in Siegen

4.1 Electrical test setup in Siegen

A dedicated test setup for electrical testing of ITkPix v1.1 and ITkPix v2 modules has been developed in Siegen [20]. It is capable of testing four pixel modules sequentially without the need for an operator to be present during testing. This is possible because of the hardware and software interlock developed for the test setup. The hardware interlock is realised via a cRIO relay card connected to the sensors in the cold box and the associated devices. For the software interlock, multiple applications are running on a Windows computer. Both interlock systems are essential to protect the pixel modules from damage during electrical testing.

Figure 4.1(a) shows the exterior of the electrical test setup. The modules are tested inside a shielded box. This shielding is necessary because a radioactive strontium-90 source with an activity of approximately 80 MBq is used for specific YARR scans. A motor inside the setup moves the source over the pixel modules. Outside of the shielded box, there is a chiller (Julabo FP51 SL) to reach and maintain stable testing temperatures for the pixel modules. A vacuum pump is connected to the setup to ensure that the pixel modules are held firmly against the cooling block. To provide the modules with low and high voltage, a low-voltage power supply (Rohde & Schwarz HMP4040) and a high-voltage power supply (Keithley 2470 SourceMeter) are used. A digital multimeter (Keithley DMM 6500) is used to read out voltages and currents of the pixel modules. Inside the shielded box, as shown in Figure 4.1(b), a cooling block made of aluminium is placed in a Styrodur cold box. On the cooling block, four custom-designed vacuum chucks are mounted. A temperature and humidity sensor is placed inside the Styrodur box to monitor the dew point. To keep the air dry, the cold box is constantly flushed with dry air to prevent condensation on the pixel modules. During electrical testing, the Styrodur box must be closed. The pixel modules are connected on the backside via a data pigtail to a data adapter card. This card is connected to the YARR readout card in the testing computer, a Linux machine. The module is read out through this connection. To power the pixel module, a second connection is needed. The power pigtail connects the modules on the front side to a power adapter card. In addition to powering the module, this connection reads out the NTC mounted on its flexible PCB.

Using this dedicated test setup, a total of ten ITkPix v1.1 and v2 modules were investigated with respect to core column issues.

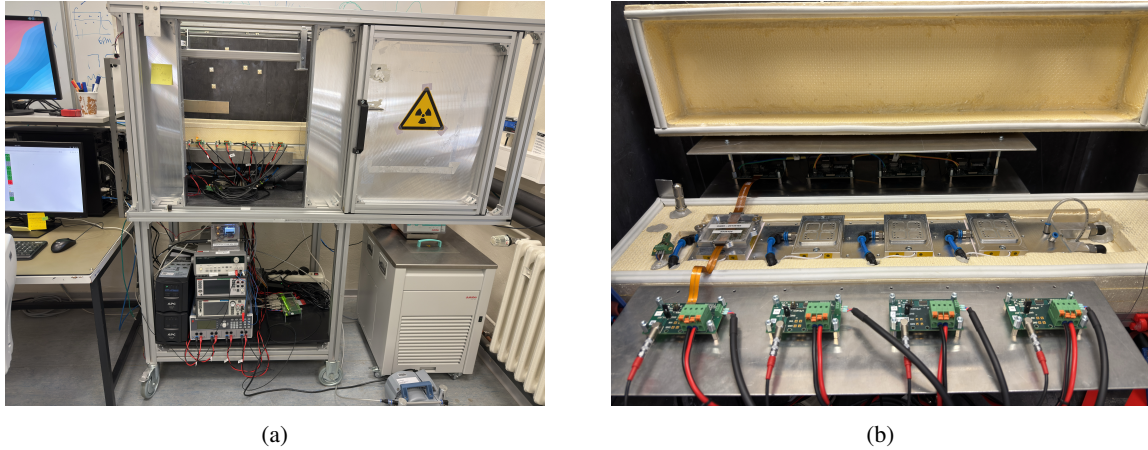


Figure 4.1: Panel (a) shows the outside of the test setup inside a shielded box. In (b), the inside of the shielded box, the cold box where modules are placed, is displayed.

4.2 Core column investigation on ITkPix v2 (RD53C) modules

During early pre-production and production of pixel modules in Siegen, the core column tools had not yet been developed. If chips showed strange patterns or could not finish electrical tests because of readout issues, they had to be turned off entirely. As both symptoms could be traced back to core column issues, these ten affected pixel modules were re-investigated using the newly developed core column tools. Four of these ten modules are equipped with ITkPix v2 (RD53C) chips: Si019, Si020, Si021, and Si022. However, they are not production modules because they were glued to a pre-production flexible PCB.

The first module to be investigated was Si019. The first step was to perform a communication check with this module after enabling all four chips in its configuration file again. A communication check is a short custom testing routine comprising an eye diagram, a core column scan, and a digital scan. The eye diagram is necessary to calibrate delay settings for all four readout lanes of the corresponding chip on the module. After that, a core column scan is used to find a core column configuration that can be used for further electrical testing. The purpose of the digital scan is that the operator is able to check whether the digital logic of the readout shows an unexpected pattern or suspicious pixels. If the operator does not observe such features on the digital-scan occupancy maps, the module is tested overnight using a full electrical test routine. In this full electrical test routine, tests are performed in warm (+20 °C NTC temperature) and cold (−15 °C NTC temperature) conditions. Module Si019 completed the communication check successfully in the warm testing regime. A plot of the digital-scan occupancy maps of all four chips is shown in Figure 4.2. The core column scan automatically masked core column 50 on chip 1 (0x20753), core columns 1 and 50 on chip 2 (0x2078d), core column 50 on chip 3 (0x20756), and core column 50 on chip 4 (0x20736). Apart from those disabled core columns, the digital scan shows the expected 100 hits on each pixel. Because of that, module Si019 underwent a full electrical test routine and passed all tests in the warm testing environment. In the cold testing regime, communication with the module could not be established. This illustrates that modules can behave differently with respect to core column issues depending on the testing temperature; further investigation was necessary. A module has independent configuration files for warm and cold testing.

Therefore, the GUI tool for manual masking was used to provide the same core column configuration for cold which was used for warm testing. After that, module Si019 could be operated without readout issues in a full electrical test routine under cold conditions. Each of those core columns introduced readout congestion when it was re-enabled. Thus, this is the core column configuration that provides stable module operation and cannot be reduced further. In the cold testing regime, almost all tests passed the given QC criteria. The failing tests are clearly not core-column-related, such as the IREF (reference current) checks included in the so-called analog readback test. Module Si019 showed five affected core columns, and after masking them with the given tools, the module could be operated as usual.

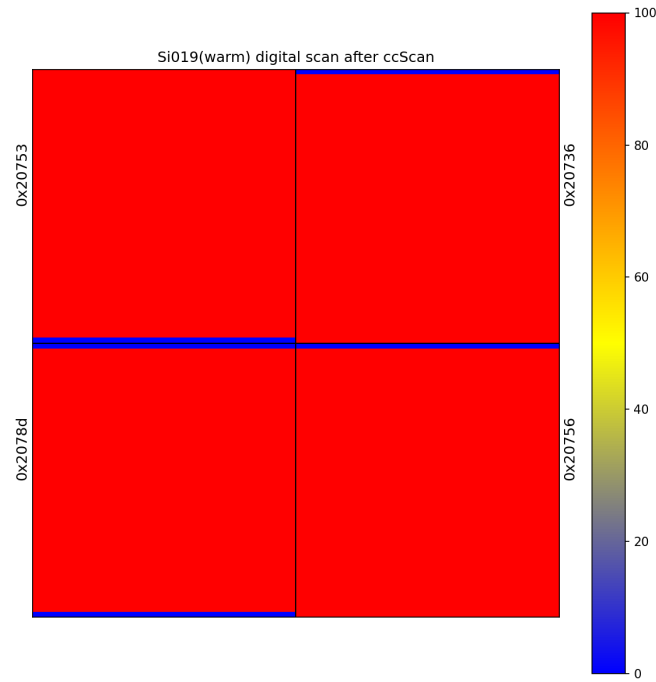


Figure 4.2: Digital-scan occupancy maps of module Si019 after a core column scan.

For the second module, Si020, a communication check was performed. The core column scan disabled core column 50 on chips 1 (0x20775) and 3 (0x207a7). After that, a few noisy and broken pixels were observed in the digital scan on the outer edges of the other two chips. During electrical testing, readout errors still occurred. The next step was to use the core column script to identify more core columns that caused those issues. The core column script did not mask any additional core columns in this case. The occupancy maps of the digital scans after the core column scan and the core column script are shown in Figure 4.3. The next step was to mask the core columns corresponding to the suspicious pixels in the digital scans manually. The GUI tool was used to disable core column 50 on chips 2 (0x20767) and 4 (0x20787). A plot of the digital scan after manual masking is displayed in Figure 4.4. All pixels outside the disabled core columns recorded the expected 100 hits. After that, the module could be operated without readout congestion. Module Si020 showed no difference in behaviour under warm and cold conditions. The module now passes all electrical tests except the IV scan, which is not related to core column issues. The IV scan measures the leakage current as a function of the applied high voltage.

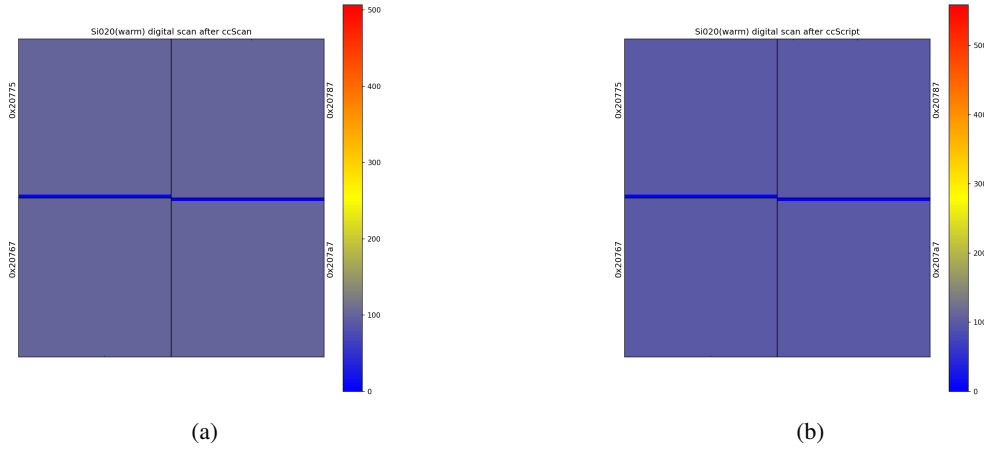


Figure 4.3: Plot (a) shows the digital-scan occupancy map of module Si020 after a core column scan. In plot (b), the digital-scan occupancy map of module Si020 after use of the core column script is displayed.

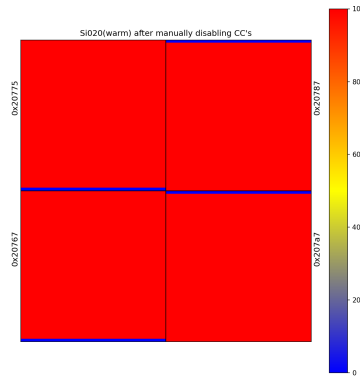


Figure 4.4: This plot shows the digital-scan occupancy maps of module Si020 after manual masking of core columns using the GUI tool.

Module Si021 had only one chip affected by core column issues, chip 3 (0x207c9). This chip showed a pattern of rubbish data, already displayed in Figure 3.1. Core columns 1 and 50 had to be masked manually, as the core column scan and script did not disable them. Thus, as for Si020, core columns required manual masking because the number of problematic pixels was below the 10% threshold implemented in the automated tools. After manual masking of those core columns, module Si021 did not show any readout congestion, and all electrical tests passed all applicable QC criteria.

The last module with an ITkPix v2 chip that was investigated in detail was module Si022. After the initial communication check, no core columns were masked automatically. In the digital-scan occupancy map shown in Figure 4.5(a), suspicious pixels were observed on chip 2 (0x2072a) and chip 4 (0x2073a). After running the core column script, core column 1 on chip 4 (0x2073a), which contained several suspicious pixels, was masked automatically. This is displayed in Figure 4.5(b). Module Si022 still showed readout issues during electrical testing, so the GUI tool was used to mask the additional core column 1 on chip 2 (0x2072a). This cleared the readout congestion during electrical testing. With this configuration, the module successfully went through a full electrical test routine under warm and cold conditions.

In summary, in the investigation of these four ITkPix v2 pre-production modules, all chips on these modules could be recovered by using the core column tools described in Chapter 3.2. This shows that core column issues can be resolved by masking a small number of affected core columns instead of disabling entire chips. All investigated modules completed most electrical tests successfully and could be operated without readout congestion. In the next section, these tools are applied to problematic ITkPix v1.1 modules, the first pre-production modules assembled in Siegen.

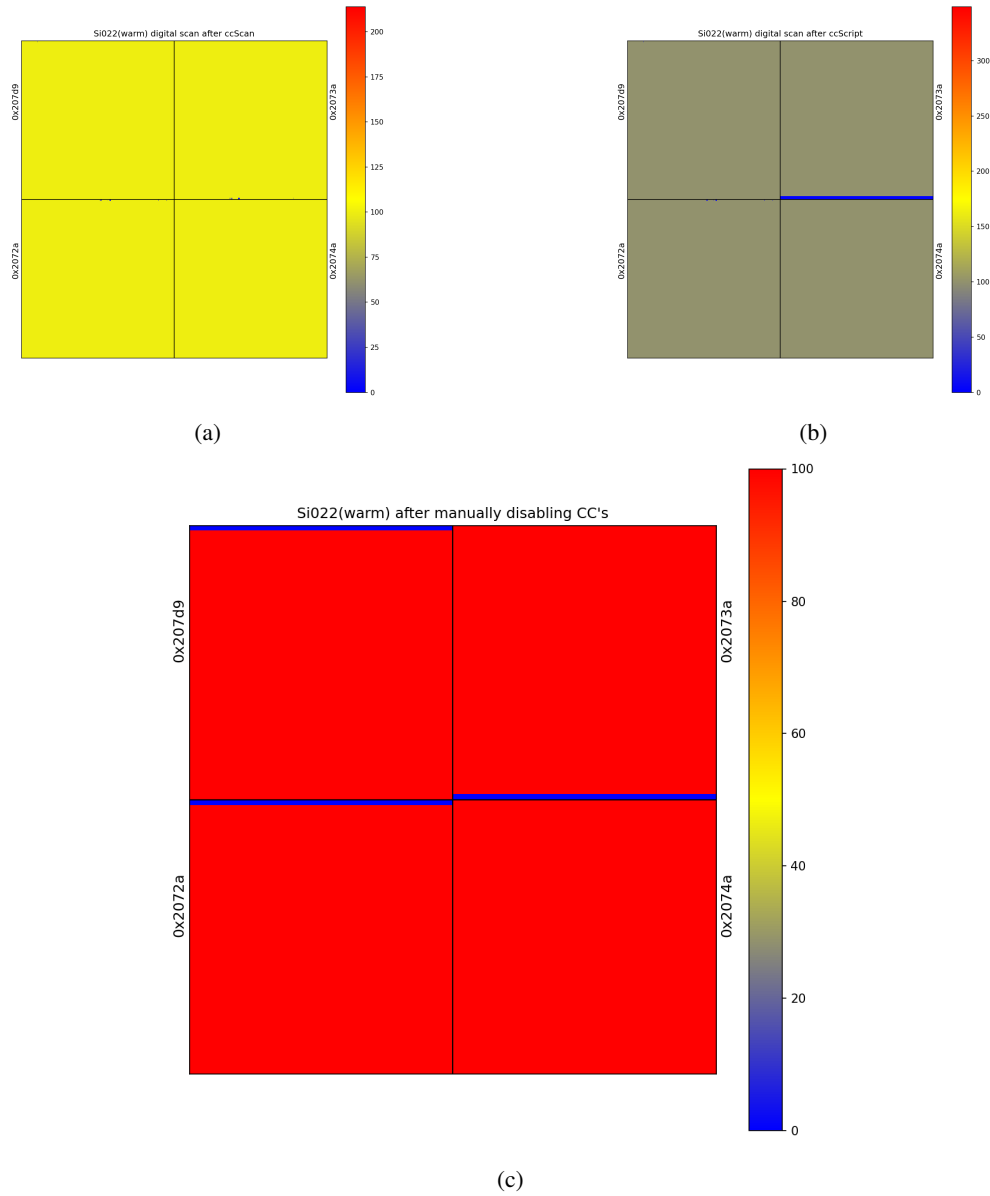


Figure 4.5: Digital-scan occupancy maps of module Si022 after different stages of the recovery procedure. (a) After the core column scan. (b) After the core column script. (c) After manual masking using the GUI tool.

4.3 Core column investigation on ITkPix v1.1 (RD53B) modules

Several ITkPix v1.1 modules contained disabled chips similar to the ITkPix v2 modules discussed above. Modules Si001, Si007, Si009, Si010, Si011 and Si012 were investigated in detail.

Module Si001 was the first ITk pixel module assembled in Siegen. The bare module was rotated relative to the flexible PCB during assembly. Because of that, the module could only be biased at 5 V instead of the intended 120 V. Because of the rotation of the components, the wire bonds touch each other and the silicon sensor. This causes a short circuit and limits the bias voltage. After the initial communication check, core column 1 on chip 2 (0x1794a) was disabled automatically. The digital-scan occupancy map is displayed in Figure 4.6. No additional manual masking was necessary. Module Si001 could be operated stably without readout issues occurring. Due to the assembly issue, the rotation of components relative to each other, the IV scan failed as expected. Apart from that, the analog readback test also failed because of the IREF checks, while the data merging test, which is not applicable to ITkPix v1.1 modules, is expected to fail.

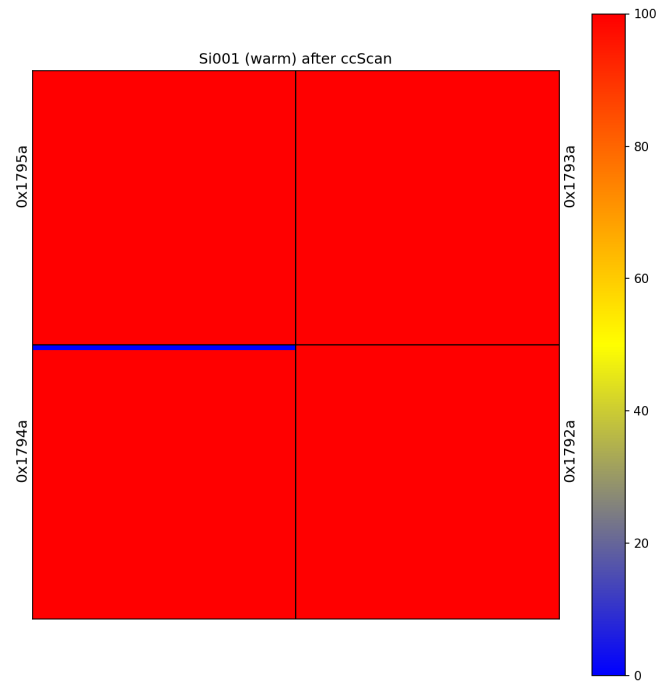


Figure 4.6: This plot shows the digital-scan occupancy map of module Si001 after a core column scan.

The next investigated module was Si007. The core column scan was able to mask core column 50 on chip 2 (0x17177) and core columns 44 and 45 on chip 4 (0x171ad). The corresponding digital-scan occupancy map is shown in Figure 4.7(a). Above the two disabled core columns on chip 4 (0x171ad) is a block of pixels that receive zero hits. Below those two core columns are multiple pixels that are noisy or broken. Module Si007 showed readout issues during electrical testing with this core column configuration. The core column script did not mask any additional core columns. Because of that, the GUI tool was used again to find a configuration through manual masking. The core column configuration after manual masking ensured stable module operation and eliminated further readout

issues. This configuration is illustrated in Figure 4.7(b). Module Si007 passes QC criteria for electrical tests except for the YARR scans. Those include a minimum health test, a tuning procedure, and a full pixel failure analysis, including a source scan. Because more than two core columns are masked on one chip, their analyses fail automatically; only two disabled core columns per chip are allowed. As for Si001, this module fails the IREF checks, while the data merging test is not applicable to ITkPix v1.1 modules and is therefore expected to fail.

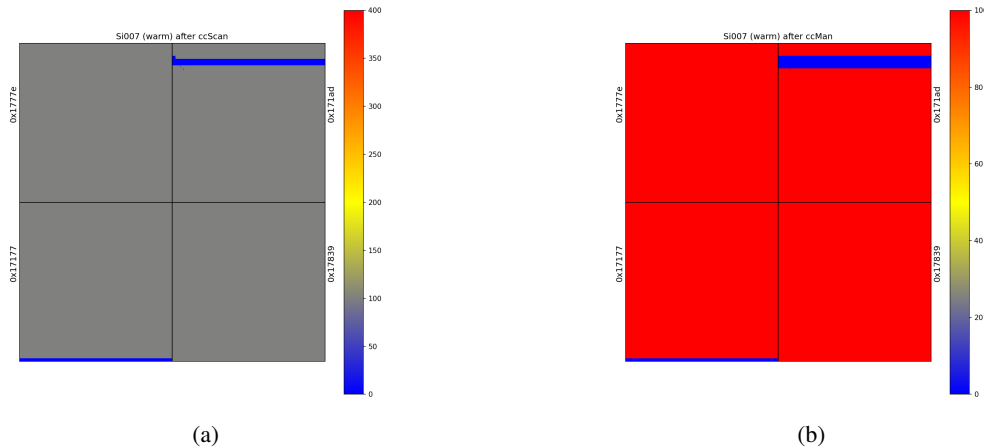


Figure 4.7: Plot (a) shows the digital-scan occupancy map of module Si007 after a core column scan. In plot (b), the digital-scan occupancy map of module Si007 after manual masking of core columns is displayed.

Module Si009 had one masked core column 45 on chip 2 (0x17859) after the initial core column scan inside the communication check. As displayed in Figure 4.8(a), some suspicious pixels are observed at the bottom edge of chip 3 (0x171ac). The module showed readout issues, which were resolved after manual masking of the corresponding core column 1 on chip 3 (0x171ac) with the GUI tool. The digital-scan occupancy map after manual masking is shown in Figure 4.8(b). The module failed only IREF checks and data merging again; otherwise, all QC criteria were satisfied and stable operation is ensured.

The next module in this investigation, Si010, had previously failed several electrical tests, with all four chips enabled. It was not possible to find a core column configuration to improve the test results of this module. A digital-scan occupancy map is displayed in Figure 4.9, where a block of pixels receives zero hits. Masking the corresponding core column did not improve electrical testing stability. The search for another working core column configuration was also unsuccessful. Therefore, the investigation for this module was discontinued.

At the beginning of the investigation of module Si011, both types of core column symptoms occurred. The digital-scan occupancy map after the initial core column scan is displayed in Figure 4.10. In Figure 4.10(a), a few pixels were very noisy, making the plot unsuitable to search for more core column issues. To identify more problematic areas, an upper display limit was set to 120 hits, and every pixel exceeding this ceiling was set to exactly 120 hits. The result is shown in Figure 4.10(b). The core column scan disabled 15 core columns (1, 3, 4, 10, 11, 13, 14, 21, 22, 23, 31, 41, 47, 48, and 49) on chip 4 (0x17557). On the other three chips, no core columns were masked automatically. A pattern of rubbish data was observed on chip 2 (0x17547), which is likely caused by more core column issues. The core column script was not useful here; it completely disabled chip 2 (0x17547).

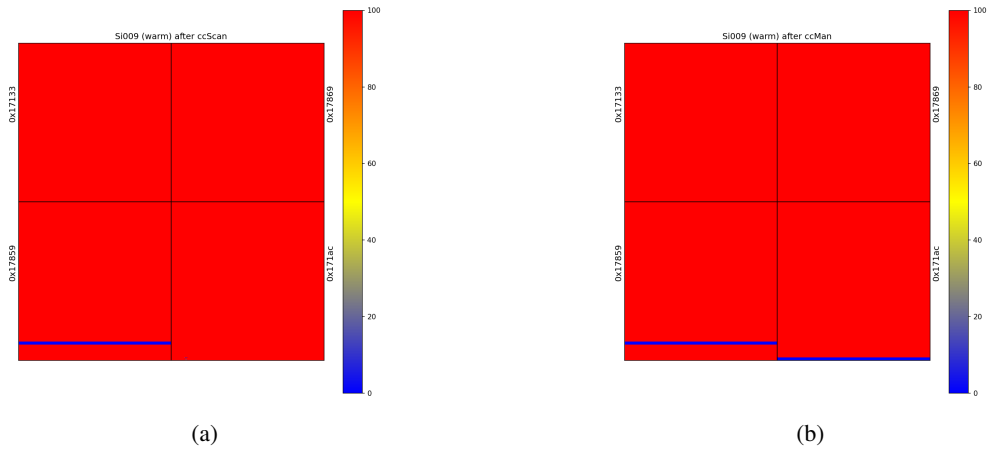


Figure 4.8: Plot (a) shows the digital-scan occupancy map of module Si009 after a core column scan. In plot (b), the digital-scan occupancy map of module Si009 after manual masking of core columns is displayed.

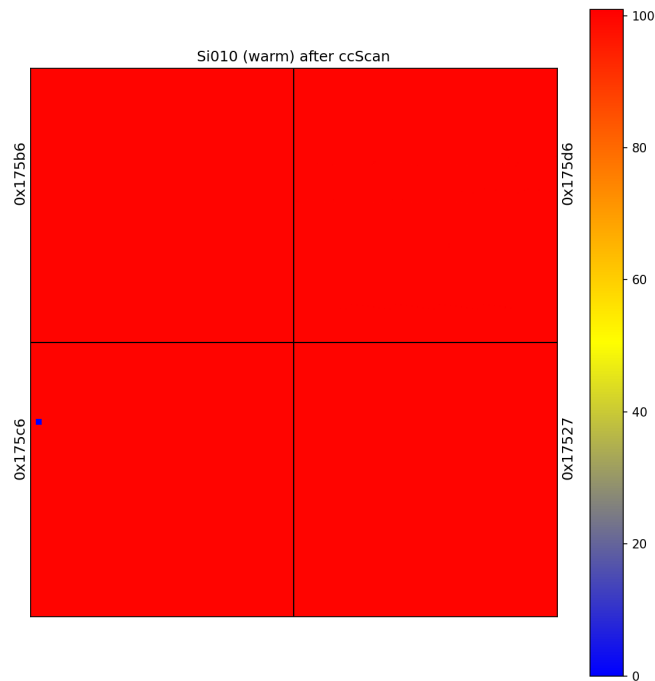


Figure 4.9: This plot shows the digital-scan occupancy maps of module Si010 after a core column scan.

Additional masking had to be done with the GUI tool. As there was no suspicious cluster of pixels on chip 2 (0x17547), different subsets of core columns were enabled and disabled until a minimal core column configuration was found to ensure stable communication with module Si011. The masked core columns were core columns 5, 6, 11, 12, 39, 40, 46, and 47 on chip 2 (0x17547) and core columns 35, 40, and 44 on chip 4 (0x17557). This configuration is displayed in Figure 4.11. It is not clear why so many core columns were problematic. No external damage was observed, but some internal circuitry may have been damaged. This may have happened because of debris between bump bonds or internal damage due to mechanical stress. This example shows that even modules with severe issues can be configured to ensure stable operation during electrical testing. This module did not pass the IREF check and failed all YARR scans as expected because of too many disabled core columns per chip.

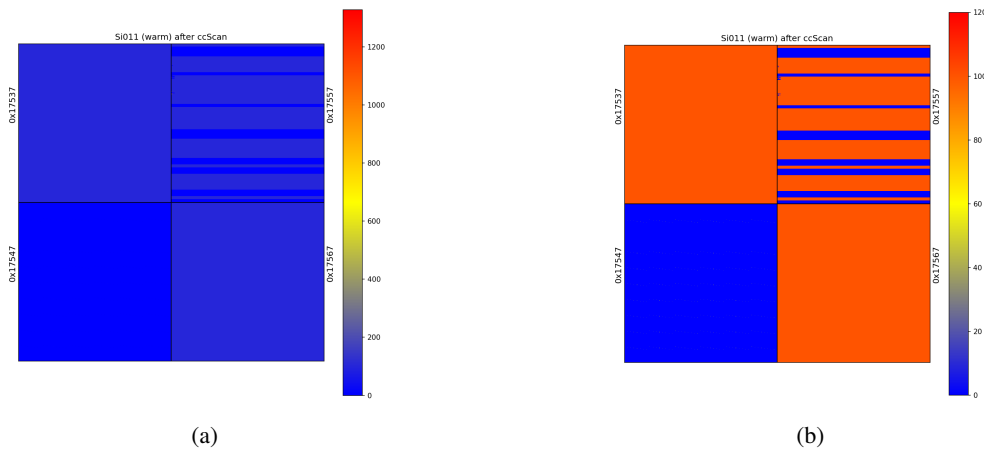


Figure 4.10: Plot (a) shows the digital-scan occupancy map of module Si011 after a core column scan. In plot (b), the same data are shown, but now every pixel with more than 120 hits is set to exactly 120 hits.

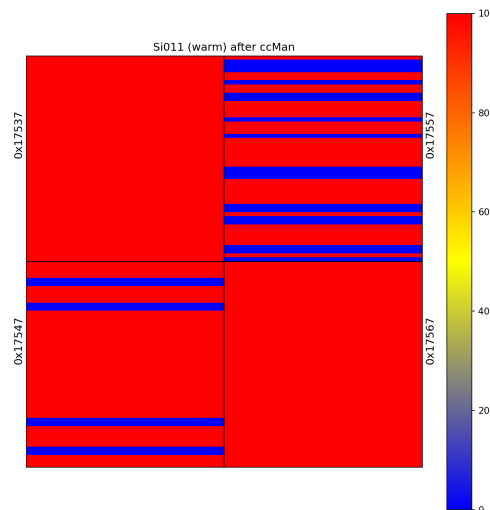


Figure 4.11: This plot shows the digital-scan occupancy maps of module Si011 after manual masking of core columns with the GUI tool.

The last investigated module in this study was Si012. Chip 2 (0x17587) was unresponsive during electrical testing. It did not show a signal in the eye diagram, which typically indicates that this chip is not recoverable. No core column configuration was found to resolve this issue, and the chip had to be disabled entirely again. The core column scan disabled core column 24 on chip 3 (0x175b7) automatically. After that, the three enabled chips could be operated stably. The digital-scan occupancy map of module Si012 is displayed in Figure 4.12. With this configuration, the module was successfully tested using the three enabled chips. A full electrical test routine passed all QC criteria except data merging, which is expected for ITkPix v1.1 modules.

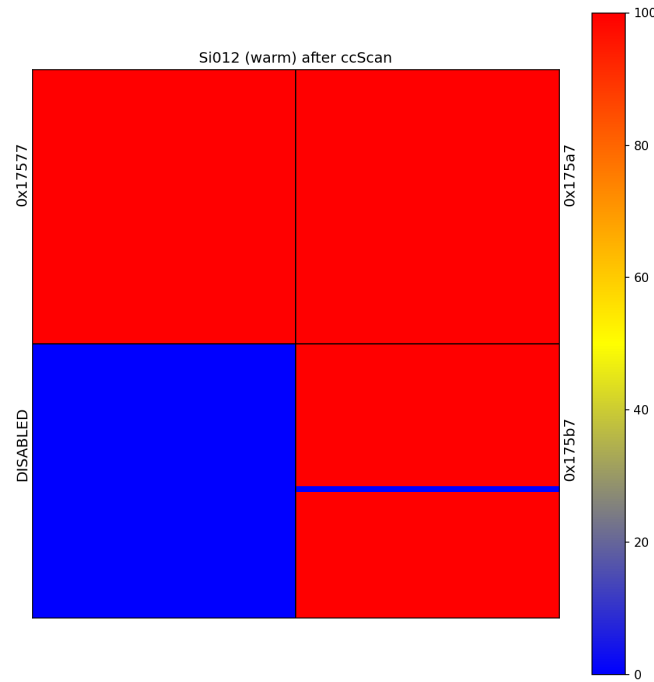


Figure 4.12: This plot shows the digital-scan occupancy maps of module Si012 after a core column scan.

In summary, of the six ITkPix v1.1 modules investigated, four (Si001, Si007, Si009, and Si011) completed full electrical test routines successfully. Similar to the study of ITkPix v2 modules, a combination of automated and manual masking tools was necessary. Some modules could be recovered by masking a small number of core columns, while others required many manually masked core columns or could not be recovered. Most investigated modules showed disabled core columns located at chip edges, which can be explained by Figure 3.3(b). This will be further investigated in Chapter 4.5.

This core column issue investigation confirms that dedicated core column tools significantly improve the fraction of modules successfully completing full electrical test routines. Based on this experience, an optimised workflow can be developed for the future treatment of both ITkPix v1.1 and v2 modules affected by core column issues.

4.4 Optimised workflow for problematic modules

The following optimised workflow is proposed for modules affected by core column issues:

An initial communication check should always be performed. After that, the digital-scan occupancy map should be carefully inspected by an operator. If no suspicious areas of noisy or broken pixels are observed, the module can undergo a full electrical test routine. In the case of suspicious pixels, a minimum health test should be done by an operator to check whether readout issues occur during this test. If this is not the case, the module can undergo a full electrical test routine. Observed readout issues should be handled in the following way: The core column script should be used to check whether additional core columns are masked automatically. If the module has additional masked core columns, it should be tested in a minimum health test again. If readout issues still occur, the operator should begin manual masking with the GUI tool. The operator should focus first on suspicious pixels in the occupancy map and mask the corresponding core columns. A minimum health test should be performed with every new configuration to check whether it is successful. This iterative process has to be done until the affected chip is recovered; otherwise, the chip must be disabled in the configuration file of the module.

4.5 Correlation of core column issues with wafer position and dicing quality

Most core column issues in Siegen have been observed at chip edges. This is consistent with the observation of L. Meng et al. [10]. To further investigate its possible connection to the dicing procedure used by hybridisation vendors, custom wafer plots were created. Most of the bare modules used for assembly in Siegen are provided by Fraunhofer IZM. To check whether disabled core columns at chip edges were adjacent on the original wafer, a custom plotting script was used to create wafer plots with the digital-scan occupancy maps of the chips. The largest group comprises 72 out of 132 chips and originated from wafer 0x233. The wafer plot is displayed in Figure 4.13. The plot clearly shows that many disabled core columns occur at adjacent chip edges. This observation supports the hypothesis that the dicing procedure used at IZM may damage the chip edges. IZM therefore introduced a new method. Laser pre-grooving is now used before the actual dicing to produce cleaner chip edges and to reduce edge defects that may lead to core column issues. Another wafer, 0x252, has been investigated to check whether the new method improves the chip quality. The wafer plot for 0x252 is shown in Figure 4.14. Of the 38 chips, only one chip was affected by a core column issue, which is located in the middle of the chip and not at the edge. Laser pre-grooving appears to improve the dicing quality of IZM significantly. This result is also visible in core column statistics for all modules built in Siegen. They are presented in Chapter 4.7.

4.5 Correlation of core column issues with wafer position and dicing quality

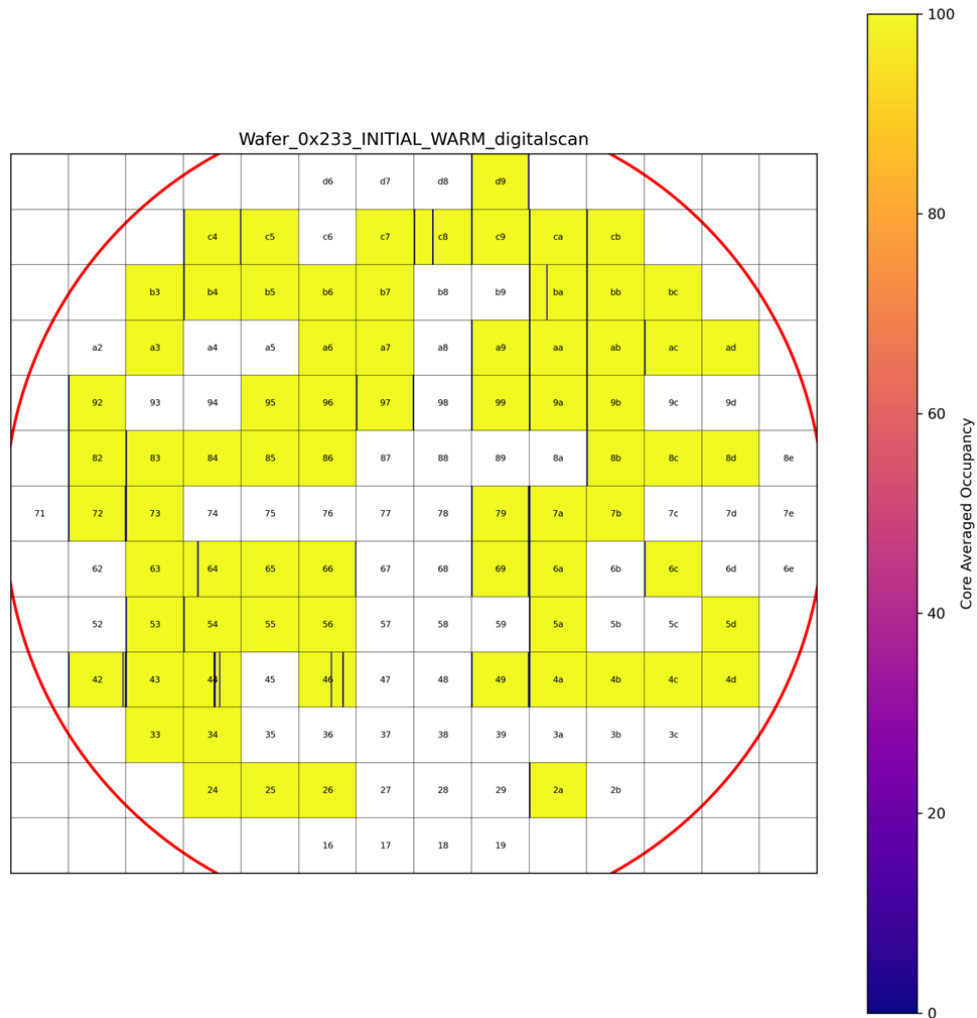


Figure 4.13: Distribution of core columns on wafer 0x233 using digital-scan occupancy maps of the chips.

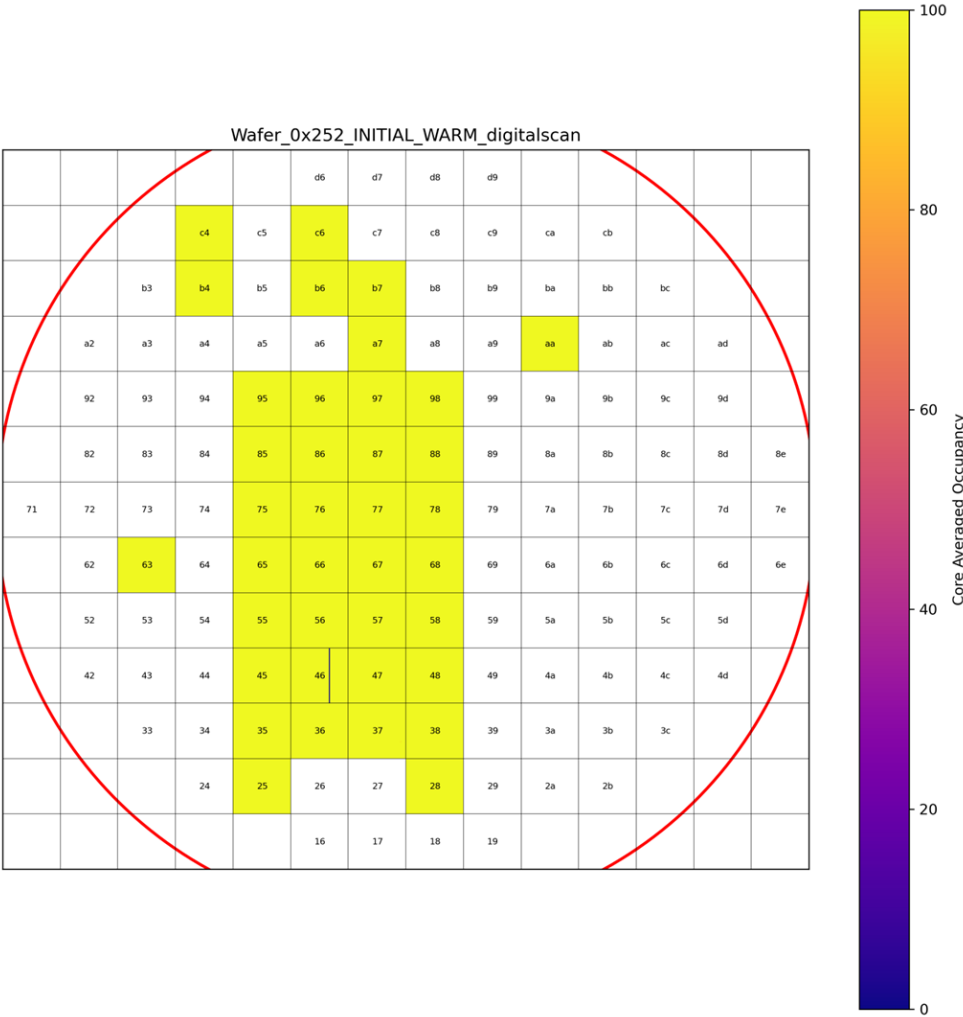


Figure 4.14: Distribution of core columns on wafer 0x252 using digital-scan occupancy maps of the chips.

4.6 Sensor cleavage

A further mechanical defect related to core column issues in this work is the so-called sensor cleavage. Because the sensor thickness is of the order of $O(100\text{ }\mu\text{m})$, it can easily be damaged if not handled carefully enough. An example of this is module Si039. The module operated without any indication of core column issues during initial electrical testing. After several mechanical processes, such as masking, shipping to industry for coating, parylene coating, shipping back to Siegen, and demasking, module Si039 showed four affected core columns. These core columns were all located in the inter-chip regions of the module. The occupancy maps before and after parylene coating are displayed in Figures 4.15(a) and 4.15(b). A photograph was taken of the chip side of the module. Between the chips, a small crack is visible in the sensor (see Figure 4.15(c)). This type of mechanical damage is referred to as sensor cleavage. Its position corresponds directly to the positions of the affected core columns on module Si039 after parylene coating.

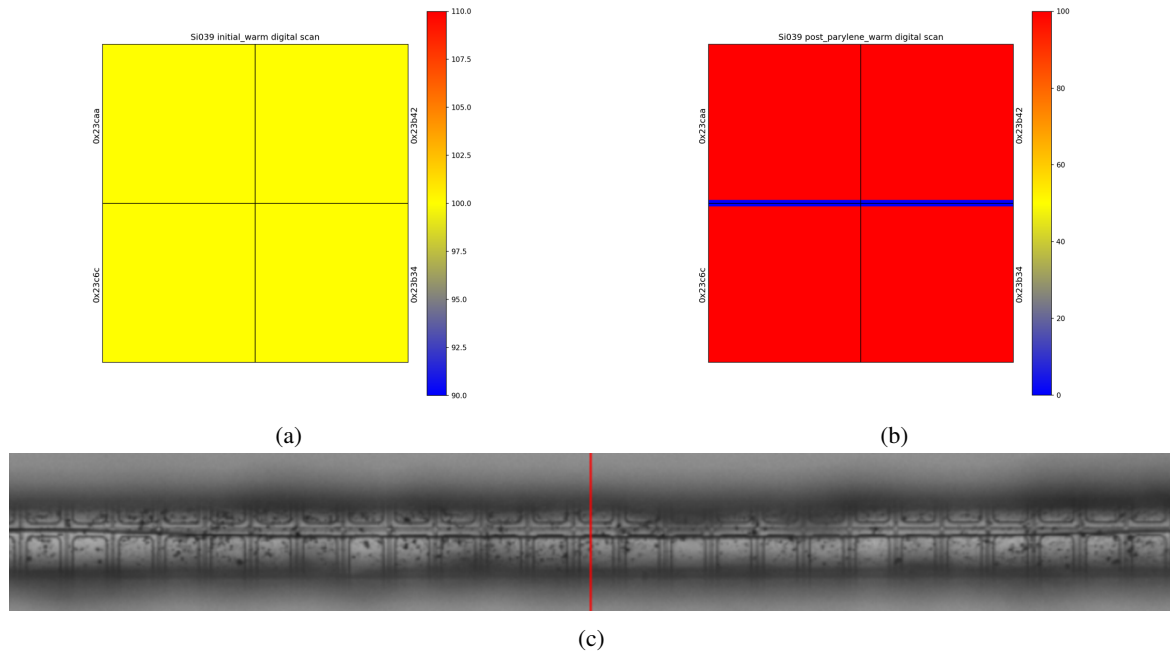


Figure 4.15: Plot (a) shows the digital-scan occupancy map of module Si039 during initial electrical testing. In plot (b), the digital-scan occupancy map of module Si039 in post-parylene electrical testing is displayed. Panel (c) shows a photograph of the mechanical damage on the silicon sensor between the FE chips.

4.7 Core column issue statistics in Siegen

Statistics for pixel modules assembled and tested in Siegen are given in Table 4.1. Modules that were damaged before initial electrical testing are excluded. Pixel modules that are currently being debugged are also excluded. The data were retrieved from the database on 12 May 2026.

The first observation is that core column issues are a significant problem in the production of ATLAS ITk pixel modules. Approximately 39% of the modules in Siegen are affected by at least one core column issue. Overall, $\approx 20\%$ of chips are affected by at least one core column issue. A second observation is that there is a strong correlation between the number of core columns at chip edges and the hybridisation vendor. The statistics for Advafab and HPK bare modules are not directly comparable to IZM owing to the limited sample size. For IZM, however, the data indicate that the introduction of the laser pre-grooving method improved the yield of modules without core column issues. Previous fractions of 75% of core column issues located at chip edges for IZM v2 modules could be reduced to $\approx 11\%$. The number of affected modules and chips is also significantly reduced because of the laser pre-grooving method. For the modules from HPK and Advafab, the observed fractions are closer to those for IZM after the introduction of laser pre-grooving.

Those observations are consistent with the wafer-based analysis presented in Chapter 4.5. They support the hypothesis that a significant fraction of core column issues originates from mechanical damage during dicing. The main findings of this work are summarised in the following chapter.

Table 4.1: Statistics of modules and chips affected by core column issues in modules assembled and tested in Siegen. Data as of 12 May 2026. The labels 'without' and 'with' refer to samples without and with laser pre-grooving, respectively.

Chip version	Vendor	Affected modules	Affected chips	Edge CCs
v1.1	IZM	6/13 ($\approx 46\%$)	9/51 ($\approx 18\%$)	4/39 ($\approx 10\%$)
v2	IZM (without)	31/56 ($\approx 55\%$)	74/221 ($\approx 34\%$)	75/100 (75%)
v2	IZM (with)	6/32 ($\approx 19\%$)	6/127 ($\approx 4.7\%$)	1/9 ($\approx 11\%$)
v2	HPK	3/13 ($\approx 23\%$)	5/51 ($\approx 9.8\%$)	1/5 (20%)
v2	Advafab	2/9 ($\approx 22\%$)	4/36 ($\approx 11\%$)	2/4 (50%)
Total	All	48/123 ($\approx 39\%$)	98/486 ($\approx 20\%$)	83/157 ($\approx 53\%$)

Conclusion

Core column issues are a significant problem in the production of ITk pixel modules. For a quad module, each masked core column corresponds to the loss of 0.5% of the module's active area. The goal of this thesis was to investigate core column issues on pixel modules tested in Siegen. Dedicated tools were evaluated, and an improved workflow was developed.

Three different tools were presented: the core column scan automatically masks severely affected core columns. The core column script improves robustness through repeated scans and implemented timeouts. If these automated tools cannot recover a module, a GUI tool can be used to mask core columns manually. Overall, no single tool is sufficient; a combination of tools is often required.

Ten ITkPix modules (six v1.1 and four v2) were investigated with respect to core column issues. Most modules could be recovered by masking a small number of core columns instead of disabling entire chips. Manual masking was needed for some severely affected modules, such as Si011. A small number of chips remained unrecoverable. Masking affected core columns significantly improves the fraction of modules that could successfully complete electrical test routines.

The origin of core column issues is not fully understood. Because of their erratic behaviour, they are difficult to classify. Core column issues at chip edges were found to depend on the hybridisation vendor. Wafer studies support this observation, as neighboring core column issues at chip edges are observed. Observations by the ATLAS Collaboration show that debris and mechanical defects can cause core column issues. The results support the hypothesis that a significant fraction of core column issues may originate from mechanical damage rather than intrinsic chip design flaws.

The dicing improvement at IZM by including laser pre-grooving in their routine reduced the number of modules affected by core column issues significantly. Before this change, $\approx 55\%$ of modules were affected ($\approx 34\%$ of chips); after introduction of the new method, the fraction of affected modules dropped to $\approx 19\%$ ($\approx 4.7\%$ at the chip level). Thus, the introduction of laser pre-grooving significantly improves module yield and reduces core column issues located at chip edges.

In future module production, the workflow developed in this thesis could enable time-efficient handling of modules affected by core column issues. The methods and observations in this work provide a practical strategy for increasing the production yield of ITk pixel modules.

Bibliography

- [1] Particle Data Group, S. Navas et al., *Review of Particle Physics*, Phys. Rev. D **110** (2024) 030001.
- [2] L. Evans and P. Bryant, *LHC Machine*, JINST **3** (2008) S08001.
- [3] ATLAS Collaboration, *The ATLAS experiment at the CERN Large Hadron Collider: a description of the detector configuration for Run 3*, JINST **19** (2024) P05063, arXiv: 2305.16623 [physics.ins-det].
- [4] ATLAS Collaboration, *The ATLAS Experiment at the CERN Large Hadron Collider*, JINST **3** (2008) S08003.
- [5] ATLAS Collaboration, *Observation of a new particle in the search for the Standard Model Higgs boson with the ATLAS detector at the LHC*, Phys. Lett. B **716** (2012) 1, arXiv: 1207.7214 [hep-ex].
- [6] CMS Collaboration, *Observation of a New Boson at a Mass of 125 GeV with the CMS Experiment at the LHC*, Phys. Lett. B **716** (2012) 30, arXiv: 1207.7235 [hep-ex].
- [7] High-Luminosity LHC Collaboration, *High-Luminosity Large Hadron Collider (HL-LHC): Technical Design Report*, CERN Yellow Reports: Monographs, Geneva: CERN, 2020.
- [8] P. Liu and on behalf of the ATLAS Collaboration, *Expected performance of the upgraded ATLAS experiment for the HL-LHC*, ATL-PHYS-PUB (2018), Physics Division, Lawrence Berkeley National Laboratory, Berkeley, CA, USA.
- [9] ATLAS Collaboration, *Technical Design Report for the ATLAS Inner Tracker Pixel Detector*, tech. rep. ATL-TDR-030, LHCC-2017-021, CERN, 2018.
- [10] L. Meng et al., *Pixel column issue in the ATLAS Inner Tracker modules*, JINST **20** (2025) C06065.
- [11] CERN, *HL-LHC Project Schedule*, URL: <https://project-hl-lhc-industry.web.cern.ch/content/project-schedule> (visited on 26/03/2026).
- [12] CERN, *New schedule for CERN's accelerators*, 2024, URL: <https://home.web.cern.ch/news/news/accelerators/new-schedule-cerns-accelerators> (visited on 02/04/2026).

- [13] G. Alimonti et al.,
RD53 pixel readout integrated circuits for ATLAS and CMS HL-LHC upgrades,
JINST **20** (2025) P03024.
- [14] ATLAS Collaboration,
Expected tracking performance of the ATLAS Inner Tracker at the High-Luminosity LHC,
JINST **20** (2025) P02018, arXiv: 2412.15090 [hep-ex].
- [15] ATLAS Collaboration and M. Saimpert, *Module development for the ATLAS ITk pixel detector*,
tech. rep. ATL-ITK-PROC-2024-018, CERN, 2024,
URL: <https://cds.cern.ch/record/2896648/>.
- [16] G. F. Knoll, *Radiation Detection and Measurement*, 4th, Hoboken: John Wiley & Sons, 2010,
ISBN: 978-0-470-13148-0.
- [17] C. Hultquist et al., *Pixel Core Column Issue in the ATLAS Inner Tracker Modules*,
PoS VERTEX2025 (2025) 014.
- [18] YARR Collaboration, *GitLab access to YARR code*, <https://gitlab.cern.ch/YARR>, 2026,
(visited on 05/06/2026).
- [19] Lawrence Berkeley National Laboratory and University of Göttingen,
PixelModuleQC: GUI tool for manual masking of ITk pixel modules,
Internal software developed within the ATLAS ITk Pixel Collaboration, 2025.
- [20] N. Malinowski, *Design and Test of an ATLAS ITk Multi-Pixel Module Test Stand*,
Master's Thesis: University of Siegen, 2024, URL:
<https://www.hep.physik.uni-siegen.de/pubs/master/malinowski-master.pdf>.

List of Figures

1.1	Overview of the LHC schedule, including the current upgrade plan to go from the LHC to the HL-LHC [11].	2
2.1	Cut-away view of the current ATLAS detector, showing its different components and their scale [4].	4
2.2	A schematic 3D longitudinal view of the ITk system, illustrating the nested barrel and end-cap structures for both the pixel (green) and strip (blue) subdetectors [14].	5
2.3	Technical r - z layouts of the ITk detector, illustrating the extended tracking coverage up to $ \eta = 4.0$. (a) Schematic view of one quadrant, showing the active elements of the pixel and strip subdetectors. (b) Detailed view of the pixel detector quadrant, highlighting the five-layer barrel layout [14].	6
2.4	Structural overview of an ITk quad pixel module. The schematic in (a) defines the layering of the internal components [15], while (b) shows the physical realisation of a module produced for the Outer Barrel.	7
2.5	Schematic of the logical data flow architecture of the RD53 chip [13]. The values for the ATLAS implementation are shown on the left in the boxes (e.g., 48 cores, 50 core columns).	9
3.1	Digital-scan occupancy maps for chip 0x207c9 of module Si021. The occupancy map in (a) is an example of a core column issue symptom: the transmission of so-called rubbish data. Panel (b) illustrates how masking problematic core columns can eliminate readout congestion and recover overall chip operation.	12
3.2	The GUI tool for manual core column masking for a single chip. The operator can view the current core column configuration or select a new set of core columns to mask manually. An occupancy map of a previous scan is displayed as a background layer to identify clusters of suspicious pixels.	15
3.3	In panel (a), a pixel module was disassembled, and debris was found between multiple bump bonds. This debris was found at a position corresponding to a disabled core column in the pixel matrix. The histogram in (b) displays the distribution of the positions of the core columns that were masked during electrical testing. Figure adapted from [10].	17
4.1	Panel (a) shows the outside of the test setup inside a shielded box. In (b), the inside of the shielded box, the cold box where modules are placed, is displayed.	20
4.2	Digital-scan occupancy maps of module Si019 after a core column scan.	21

4.3	Plot (a) shows the digital-scan occupancy map of module Si020 after a core column scan. In plot (b), the digital-scan occupancy map of module Si020 after use of the core column script is displayed.	22
4.4	This plot shows the digital-scan occupancy maps of module Si020 after manual masking of core columns using the GUI tool.	22
4.5	Digital-scan occupancy maps of module Si022 after different stages of the recovery procedure. (a) After the core column scan. (b) After the core column script. (c) After manual masking using the GUI tool.	24
4.6	This plot shows the digital-scan occupancy map of module Si001 after a core column scan.	25
4.7	Plot (a) shows the digital-scan occupancy map of module Si007 after a core column scan. In plot (b), the digital-scan occupancy map of module Si007 after manual masking of core columns is displayed.	26
4.8	Plot (a) shows the digital-scan occupancy map of module Si009 after a core column scan. In plot (b), the digital-scan occupancy map of module Si009 after manual masking of core columns is displayed.	27
4.9	This plot shows the digital-scan occupancy maps of module Si010 after a core column scan.	27
4.10	Plot (a) shows the digital-scan occupancy map of module Si011 after a core column scan. In plot (b), the same data are shown, but now every pixel with more than 120 hits is set to exactly 120 hits.	28
4.11	This plot shows the digital-scan occupancy maps of module Si011 after manual masking of core columns with the GUI tool.	28
4.12	This plot shows the digital-scan occupancy maps of module Si012 after a core column scan.	29
4.13	Distribution of core columns on wafer 0x233 using digital-scan occupancy maps of the chips.	31
4.14	Distribution of core columns on wafer 0x252 using digital-scan occupancy maps of the chips.	32
4.15	Plot (a) shows the digital-scan occupancy map of module Si039 during initial electrical testing. In plot (b), the digital-scan occupancy map of module Si039 in post-parylene electrical testing is displayed. Panel (c) shows a photograph of the mechanical damage on the silicon sensor between the FE chips.	33

List of Tables

3.1 Published statistics of modules and chips affected by core column issues, extracted from the ITk production database by L. Meng et al.. The warm testing regime is around +20 °C and cold testing around –15 °C module NTC temperature. Adapted from Ref. [10]. 16

4.1 Statistics of modules and chips affected by core column issues in modules assembled and tested in Siegen. Data as of 12 May 2026. The labels 'without' and 'with' refer to samples without and with laser pre-grooving, respectively. 34